Control (638-6065-001)

Rockwell International

instructions

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1. DESCRIPTION

Control 638-6065-001, shown in figure 1, is a 2-layer planar card with a 130-pin edge-on connector (2 layers, 65 pins each).

The control card consists of vbfo/operating frequency variable clock generator, parallel storage registers for the operating frequency signal, bcd parallel frequency band and 1/2-octave control circuits, tune start control circuit, and monitor control circuits.

(To Be Supplied)

Control
Figure 1

2. PRINCIPLES OF OPERATION

2.1 General

The control card:

a. Receives operating frequency rate control information and generates/stores the data for the operating frequency selected.

b. Receives vbfo rate control information and supplies a variable clock signal for the vbfo circuit card.

c. Uses the parallel bcd signals to produce frequency band control outputs.

d. Uses a fault summary circuit to summarize a power supply fault, a synthesizer fault, and a vbfo synthesizer fault to produce a receiver fault indication.

e. Uses an rf overload summary circuit to summarize a preselector rf overload and a receiver rf overload and produce a receive rf overload indication.

f. Receives a preselector fault signal and supplies a buffered/current driven preselector fault indication.

g. Receives a local frequency change signal, a remote frequency change signal, or a change in local enable signal and produces a tune start pulse output.

2.2 Rate Control to Variable Clock Circuit

(Refer to figure 2.)

The rate control to variable clock circuit consists of a PROM (programmable read-only memory), a clock generator, a preset divide-by-N counter, and a coarse tune and a fine tune multiplexer/demultiplexer.

The clock generator (U1A, U1B, and U6-Q3 output) provides a tuning clock of 13 250 Hz. Binary counter/divider U6 provides outputs which are binary multiples of the clock generator output. The selected change rate is determined by the bcd rate input, PROM U25, and the coarse tune and fine tune multiplexer/demultiplexers (U24, U7). Note that PROM U25 has 8 address inputs. Address inputs 0 through 4 are rate code inputs. Address inputs 5 through 7 are control functions. Table 1 shows the input address for the control functions. Tables 2 through 9 show the input address for the rate code inputs and the associated output division ratios-from the multiplexer/demultiplexer circuit.

2.3 Vbfo Clock Output

The vbfo clock output is supplied when a vbfo tune input is applied (logic 1) and rate control inputs are applied. AND gate U11D is enabled and the variable clock is supplied through U11D and U11C to the vbfo clock out at P1-85.

Note the $\overline{\text{clock inhibit}}$ (logic 1) must be applied to enable gate U11C.

2.4 Bcd Frequency Control Outputs (Refer to figure 2.)

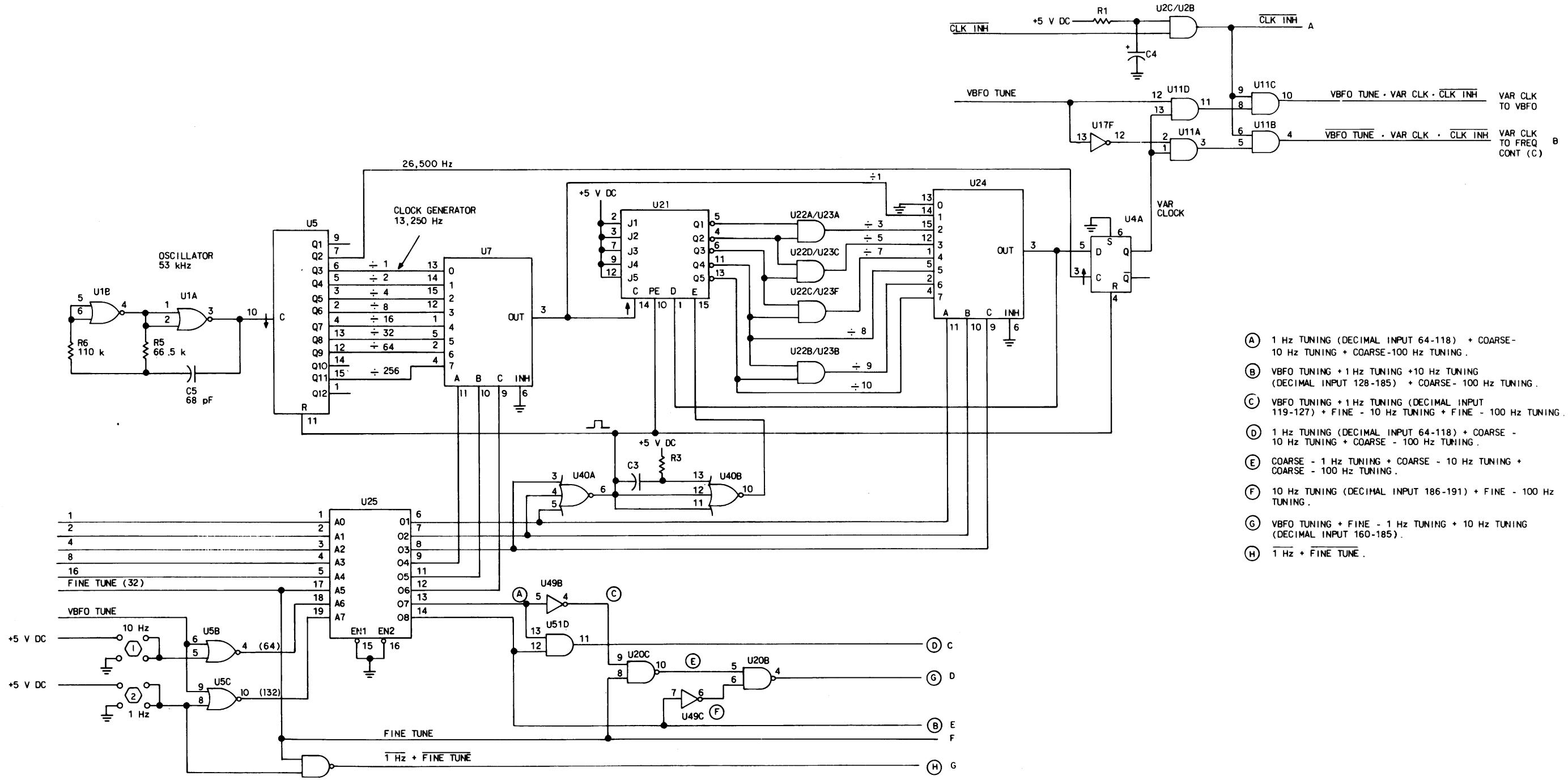
The frequency control circuits are rate-of-change frequency control input signals to parallel bcd frequency control output signals. Bcd output signals for 1 Hz to 30 MHz in 1-Hz steps are provided when used with the correct rate inputs and strapping. Current driven outputs for 1 kHz to 30 MHz are also supplied to be used with an associated preselector. Band control output circuits or 1/2-octave control outputs are also provided when used with the appropriate strapping and associated rf translator.

2.4.1 Band Control Output Circuits (Refer to figure 3.)

When strapped for standard filter control (SF), the band control output circuits receive parallel bcd input control signals (from storage registers U29-U36) and converts them to one-of-three band control output signals. Frequency ranges of the bands are as follows: band 1 - 0 to 539 kHz, band 2 - 540 kHz to 1.59 MHz, and band 3 - 1.60 to 29.99 MHz. Refer to figure 3 and note that any bcd frequency input that is between the low frequency of one band and the low frequency of the next higher band provides the associated band output control signal (logic 0 = enabled).

Table 1. PROM U25, Address Inputs for Control Functions.

CONTROL FUNCTION	LOGIC INPUTS		
	5	6	7
Vbfo -- coarse tuning	0	0	0
Vbfo -- fine tuning	1	0	0
Frequency -- coarse 1-Hz tuning	0	1	0
Frequency -- fine 1-Hz tuning	1	1	0
Frequency -- coarse 10-Hz tuning	0	0	1
Frequency -- fine 10-Hz tuning	1	0	1
Frequency -- coarse 100-Hz tuning	0	1	1
Frequency -- fine 100-Hz tuning	1	1	1



(A) 1 Hz TUNING (DECIMAL INPUT 64-118) + COARSE - 10 Hz TUNING + COARSE - 100 Hz TUNING.

(B) VBFO TUNING + 1 Hz TUNING + 10 Hz TUNING (DECIMAL INPUT 128-185) + COARSE - 100 Hz TUNING.

(C) VBFO TUNING + 1 Hz TUNING (DECIMAL INPUT 119-127) + FINE - 10 Hz TUNING + FINE - 100 Hz TUNING.

(D) 1 Hz TUNING (DECIMAL INPUT 64-118) + COARSE - 10 Hz TUNING + COARSE - 100 Hz TUNING.

(E) COARSE - 1 Hz TUNING + COARSE - 10 Hz TUNING + COARSE - 100 Hz TUNING.

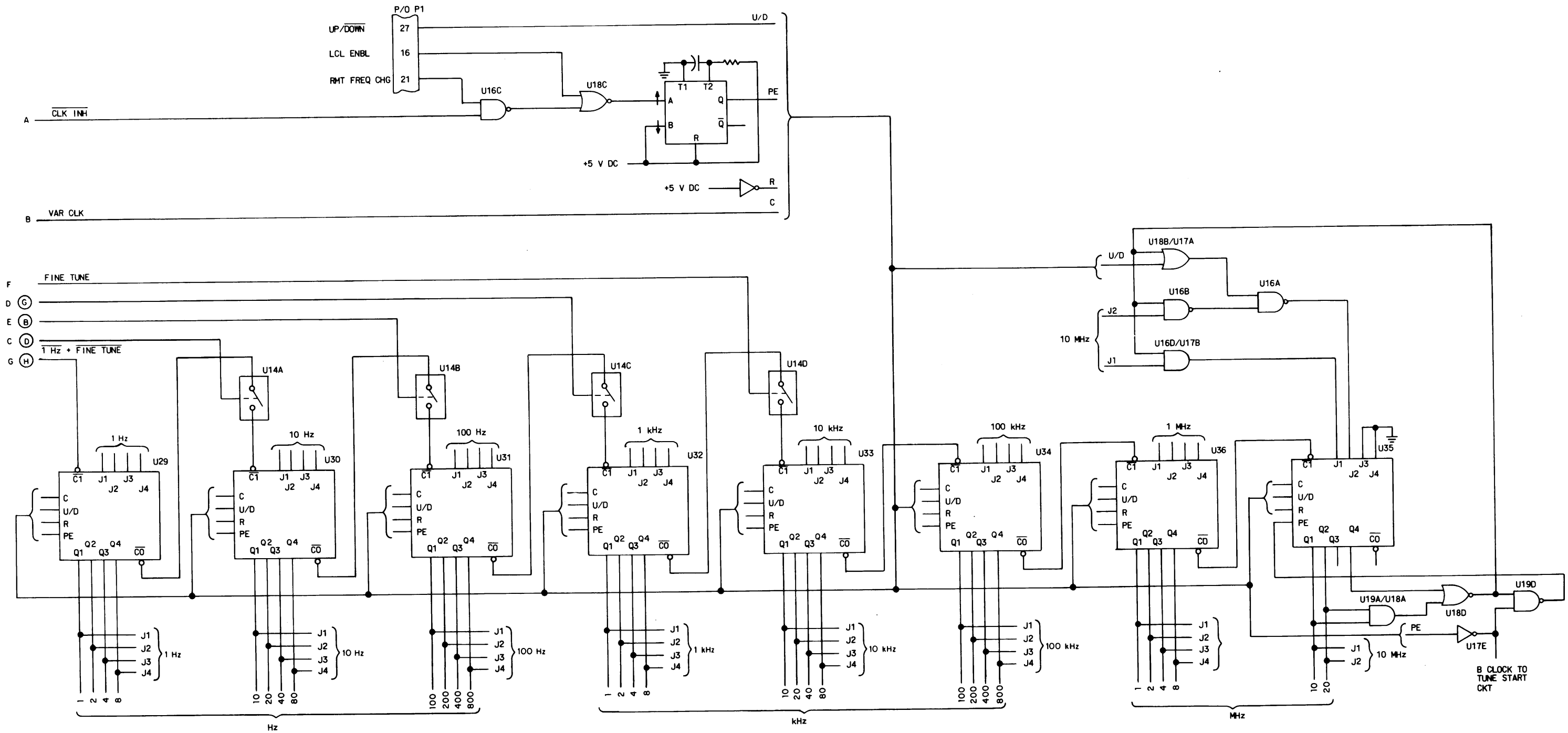
(F) 10 Hz TUNING (DECIMAL INPUT 186-191) + FINE - 100 Hz TUNING.

(G) VBFO TUNING + FINE - 1 Hz TUNING + 10 Hz TUNING (DECIMAL INPUT 160-185).

(H) $\overline{1\text{ Hz}} + \overline{\text{FINE TUNE}}$.

TPA-1257-024

Rate Control to Variable Clock and Frequency Control Circuit
Figure 2 (Sheet 1 of 2)



TPA-1257-024

Rate Control to Variable Clock and Frequency Control Circuit
Figure 2 (Sheet 2)

Table 2. PROM U25, VBFO — Coarse Tuning.

DECIMAL INPUT	PROM U25																	U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS									IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																			
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8		A	B	C		A	B	C			
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1		1	1	1	7	0	0	0	0	NONE	0
1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1		1	1	1	7	1	1	1	7	2560	5
2	0	1	0	0	0	0	0	0	1	1	1	0	1	1	0	1		0	1	1	6	1	1	1	7	640	21
3	1	1	0	0	0	0	0	0	1	1	1	1	0	1	0	1		1	0	1	5	1	1	1	7	320	41
4	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1		1	0	1	5	0	0	1	4	224	59
5	1	0	1	0	0	0	0	0	1	1	1	0	0	1	0	1		0	0	1	4	1	1	1	7	160	83
6	0	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1		0	0	1	4	1	0	1	5	128	104
7	1	1	1	0	0	0	0	0	0	0	1	0	0	1	0	1		0	0	1	4	0	0	1	4	112	118
8	0	0	0	1	0	0	0	0	0	1	0	1	0	1	0	1		1	0	1	5	0	1	0	2	96	138
9	1	0	0	1	0	0	0	0	1	1	1	1	1	0	0	1		1	1	0	3	1	1	1	7	80	166
10	0	1	0	1	0	0	0	0	0	1	1	1	1	0	0	1		1	1	0	3	0	1	1	6	72	184
11	1	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1		1	1	0	3	1	0	1	5	64	207
12	0	0	1	1	0	0	0	0	0	0	1	1	1	0	0	1		1	1	0	3	0	0	1	4	56	237
13	1	0	1	1	0	0	0	0	0	1	0	0	0	1	0	1		0	0	1	4	0	1	0	2	48	276
14	0	1	1	1	0	0	0	0	1	1	1	0	1	0	0	1		0	1	0	2	1	1	1	7	40	331
15	1	1	1	1	0	0	0	0	0	1	1	0	1	0	0	1		0	1	0	2	0	1	1	6	36	368
16	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1		0	1	0	2	1	0	1	5	32	414
17	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	1		0	1	0	2	0	0	1	4	28	473
18	0	1	0	0	1	0	0	0	0	1	0	1	1	0	0	1		1	1	0	3	0	1	0	2	24	552
19	1	1	0	0	1	0	0	0	0	1	0	1	1	0	0	1		1	1	0	3	0	1	0	2	24	552
20	0	0	1	0	1	0	0	0	1	1	1	1	0	0	0	1		1	0	0	1	1	1	1	7	20	663
21	1	0	1	0	1	0	0	0	0	1	1	1	0	0	0	1		1	0	0	1	0	1	1	6	18	736
22	0	1	1	0	1	0	0	0	1	0	1	1	0	0	0	1		1	0	0	1	1	0	1	5	16	828
23	1	1	1	0	1	0	0	0	0	0	1	1	0	0	0	1		1	0	0	1	0	0	1	4	14	946
24	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
25	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
26	0	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
27	1	1	0	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
28	0	0	1	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
29	1	0	1	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
30	0	1	1	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
31	1	1	1	1	1	0	0	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104

Table 3. PROM U25, VBFO — Fine Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
32	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	1	1	1	7	0	0	0	0	NONE	0
33	1	0	0	0	0	1	0	0	1	1	1	1	1	1	0	1	1	1	1	7	1	1	1	7	2560	5
34	0	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1	0	1	1	6	1	1	1	7	640	21
35	1	1	0	0	0	1	0	0	1	1	1	1	0	1	0	1	1	0	1	5	1	1	1	7	320	41
36	0	0	1	0	0	1	0	0	0	0	1	1	0	1	0	1	1	0	1	5	0	0	1	4	224	59
37	1	0	1	0	0	1	0	0	1	1	1	0	0	1	0	1	0	0	1	4	1	1	1	7	160	83
38	0	1	1	0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	4	1	0	1	5	128	104
39	1	1	1	0	0	1	0	0	0	0	1	0	0	1	0	1	0	0	1	4	0	0	1	4	112	118
40	0	0	0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	0	1	5	0	1	0	2	96	138
41	1	0	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	1	0	3	1	1	1	7	80	166
42	0	1	0	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	0	3	0	1	1	6	72	184
43	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	1	1	0	3	1	0	1	5	64	207
44	0	0	1	1	0	1	0	0	0	0	1	1	1	0	0	1	1	1	0	3	0	0	1	4	56	237
45	1	0	1	1	0	1	0	0	0	1	0	0	0	1	0	1	0	0	1	4	0	1	0	2	48	276
46	0	1	1	1	0	1	0	0	1	1	1	0	1	0	0	1	0	1	0	2	1	1	1	7	40	331
47	1	1	1	1	0	1	0	0	0	1	1	0	1	0	0	1	0	1	0	2	0	1	1	6	36	368
48	0	0	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	1	0	2	1	0	1	5	32	414
49	1	0	0	0	1	1	0	0	0	0	1	0	1	0	0	1	0	1	0	2	0	0	1	4	28	473
50	0	1	0	0	1	1	0	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
51	1	1	0	0	1	1	0	0	0	1	0	1	1	0	0	1	1	1	0	3	0	1	0	2	24	552
52	0	0	1	0	1	1	0	0	1	1	1	1	0	0	0	1	1	0	0	1	1	1	1	7	20	663
53	1	0	1	0	1	1	0	0	0	1	1	1	0	0	0	1	1	0	0	1	0	1	1	6	18	736
54	0	1	1	0	1	1	0	0	1	0	1	1	0	0	0	1	1	0	0	1	1	0	1	5	16	828
55	1	1	1	0	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	1	4	14	946
56	0	0	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
57	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
58	0	1	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
59	1	1	0	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
60	0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
61	1	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
62	0	1	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104
63	1	1	1	1	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	2	0	1	0	2	12	1104

Table 4. PROM U25, Frequency — Coarse 1-Hz Tuning.

DECIMAL INPUT	PROM U25																	U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS									IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																			
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8		A	B	C		A	B	C			
64	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1		1	1	1	7	0	0	0	0	NONE	0
65	1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1		1	1	1	7	1	1	1	7	2560	5
66	0	1	0	0	0	0	1	0	1	1	1	0	1	1	1	1		0	1	1	6	1	1	1	7	640	21
67	1	1	0	0	0	0	1	0	1	1	1	1	0	1	1	1		1	0	1	5	1	1	1	7	320	41
68	0	0	1	0	0	0	1	0	0	0	1	1	0	1	1	1		1	0	1	5	0	0	1	4	224	59
69	1	0	1	0	0	0	1	0	1	1	1	0	0	1	1	1		0	0	1	4	1	1	1	7	160	83
70	0	1	1	0	0	0	1	0	1	0	1	0	0	1	1	1		0	0	1	4	1	0	1	5	128	104
71	1	1	1	0	0	0	1	0	0	0	1	0	0	1	1	1		0	0	1	4	0	0	1	4	112	118
72	0	0	0	1	0	0	1	0	0	1	0	1	0	1	1	1		1	0	1	5	0	1	0	2	96	138
73	1	0	0	1	0	0	1	0	1	1	1	1	1	0	1	1		1	1	0	3	1	1	1	7	80	166
74	0	1	0	1	0	0	1	0	0	1	1	1	1	0	1	1		1	1	0	3	0	1	1	6	72	184
75	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1	1		1	1	0	3	1	0	1	5	64	207
76	0	0	1	1	0	0	1	0	0	0	1	1	1	0	1	1		1	1	0	3	0	0	1	4	56	237
77	1	0	1	1	0	0	1	0	0	1	0	0	0	1	1	1		0	0	1	4	0	1	0	2	48	276
78	0	1	1	1	0	0	1	0	1	1	1	0	1	0	1	1		0	1	0	2	1	1	1	7	40	331
79	1	1	1	1	0	0	1	0	0	1	1	0	1	0	1	1		0	1	0	2	0	1	1	6	36	368
80	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	1		0	1	0	2	1	0	1	5	32	414
81	1	0	0	0	1	0	1	0	0	0	1	0	1	0	1	1		0	1	0	2	0	0	1	4	28	473
82	0	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1		1	1	0	3	0	1	0	2	24	552
83	1	1	0	0	1	0	1	0	0	1	0	1	1	0	1	1		1	1	0	3	0	1	0	2	24	552
84	0	0	1	0	1	0	1	0	1	1	1	1	0	0	1	1		1	0	0	1	1	1	1	7	20	663
85	1	0	1	0	1	0	1	0	0	1	1	1	0	0	1	1		1	0	0	1	0	1	1	6	18	736
86	0	1	1	0	1	0	1	0	1	0	1	1	0	0	1	1		1	0	0	1	1	0	1	5	16	828
87	1	1	1	0	1	0	1	0	0	0	1	1	0	0	1	1		1	0	0	1	0	0	1	4	14	946
88	0	0	0	1	1	0	1	0	0	1	0	0	1	0	1	1		0	1	0	2	0	1	0	2	12	1104
89	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1	1		1	0	0	1	1	1	0	3	10	1325
90	0	1	0	1	1	0	1	0	1	0	0	1	1	0	1	1		1	1	0	3	1	0	0	1	8	1656
91	1	1	0	1	1	0	1	0	0	1	0	1	0	0	1	1		1	0	0	1	0	1	0	2	6	2208
92	0	0	1	1	1	0	1	0	0	1	0	1	0	0	1	1		1	0	0	1	0	1	0	2	6	2208
93	1	0	1	1	1	0	1	0	0	1	0	1	0	0	1	1		1	0	0	1	0	1	0	2	6	2208
94	0	1	1	1	1	0	1	0	0	1	0	1	0	0	1	1		1	0	0	1	0	1	0	2	6	2208
95	1	1	1	1	1	0	1	0	0	1	0	1	0	0	1	1		1	0	0	1	0	1	0	2	6	2208

Table 5. PROM U25, Frequency — Fine 1-Hz Tuning.

DECIMAL INPUT	PROM U25																	U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS									IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																			
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8		A	B	C		A	B	C			
96	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1		1	1	1	7	0	0	0	0	NONE	0
97	1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1		1	1	1	7	1	1	1	7	2560	5
98	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	1		0	1	1	6	1	1	1	7	640	21
99	1	1	0	0	0	1	1	0	1	1	1	1	0	1	1	1		1	0	1	5	1	1	1	7	320	41
100	0	0	1	0	0	1	1	0	0	0	1	1	0	1	1	1		1	0	1	5	0	0	1	4	224	59
101	1	0	1	0	0	1	1	0	1	1	1	0	0	1	1	1		0	0	1	4	1	1	1	7	160	83
102	0	1	1	0	0	1	1	0	1	0	1	0	0	1	1	1		0	0	1	4	1	0	1	5	128	104
103	1	1	1	0	0	1	1	0	0	0	1	0	0	1	1	1		0	0	1	4	0	0	1	4	112	118
104	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	1		1	0	1	5	0	1	0	2	96	138
105	1	0	0	1	0	1	1	0	1	1	1	1	1	0	1	1		1	1	0	3	1	1	1	7	80	166
106	0	1	0	1	0	1	1	0	0	1	1	1	1	0	1	1		1	1	0	3	0	1	1	6	72	184
107	1	1	0	1	0	1	1	0	1	0	1	1	1	0	1	1		1	1	0	3	1	0	1	5	64	207
108	0	0	1	1	0	1	1	0	0	0	1	1	1	0	1	1		1	1	0	3	0	0	1	4	56	237
109	1	0	1	1	0	1	1	0	0	1	0	0	0	1	1	1		0	0	1	4	0	1	0	2	48	276
110	0	1	1	1	0	1	1	0	1	1	1	0	1	0	1	1		0	1	0	2	1	1	1	7	40	331
111	1	1	1	1	0	1	1	0	0	1	1	0	1	0	1	1		0	1	0	2	0	1	1	6	36	368
112	0	0	0	0	1	1	1	0	1	0	1	0	1	0	1	1		0	1	0	2	1	0	1	5	32	414
113	1	0	0	0	1	1	1	0	0	0	1	0	1	0	1	1		0	1	0	2	0	0	1	4	28	473
114	0	1	0	0	1	1	1	0	0	1	0	1	1	0	1	1		1	1	0	3	0	1	0	2	24	552
115	1	1	0	0	1	1	1	0	1	1	1	1	0	0	1	1		1	0	0	1	1	1	1	7	20	663
116	0	0	1	0	1	1	1	0	1	0	1	1	0	0	1	1		1	0	0	1	1	0	1	5	16	828
117	1	0	1	0	1	1	1	0	0	0	1	1	0	0	1	1		1	0	0	1	0	0	1	4	14	946
118	0	1	1	0	1	1	1	0	1	1	0	1	0	0	1	1		1	0	0	1	1	1	0	3	10	1325
119	1	1	1	0	1	1	1	0	1	1	1	1	1	0	0	1		1	1	0	3	1	1	1	7	80	166
120	0	0	0	1	1	1	1	0	1	0	1	1	1	0	0	1		1	1	0	3	1	0	1	5	64	207
121	1	0	0	1	1	1	1	0	0	1	0	0	0	1	0	1		0	0	1	4	0	1	0	2	48	276
122	0	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1		0	1	0	2	0	1	1	6	36	368
123	1	1	0	1	1	1	1	0	0	1	0	1	1	0	0	1		1	1	0	3	0	1	0	2	24	552
124	0	0	1	1	1	1	1	0	0	1	1	1	0	0	0	1		1	0	0	1	0	1	1	6	18	736
125	1	0	1	1	1	1	1	0	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
126	0	1	1	1	1	1	1	0	1	0	0	1	1	0	0	1		1	1	0	3	1	0	0	1	8	1656
127	1	1	1	1	1	1	1	0	0	1	0	1	0	0	0	1		1	0	0	1	0	1	0	2	6	2208

Table 6. PROM U25, Frequency — Coarse 10-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
128	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	7	0	0	0	0	NONE	0
129	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	7	1	1	1	7	2560	5
130	0	1	0	0	0	0	0	1	1	1	1	0	1	1	1	1	0	1	1	6	1	1	1	7	640	21
131	1	1	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	5	1	1	1	7	320	41
132	0	0	1	0	0	0	0	1	0	0	1	1	0	1	1	1	1	0	1	5	0	0	1	4	224	59
133	1	0	1	0	0	0	0	1	1	1	1	0	0	1	1	1	0	0	1	4	1	1	1	7	160	83
134	0	1	1	0	0	0	0	1	1	0	1	0	0	1	1	1	0	0	1	4	1	0	1	5	128	104
135	1	1	1	0	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1	4	0	0	1	4	112	118
136	0	0	0	1	0	0	0	1	0	1	0	1	0	1	1	1	1	0	1	5	0	1	0	2	96	138
137	1	0	0	1	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0	3	1	1	1	7	80	166
138	0	1	0	1	0	0	0	1	0	1	1	1	1	0	1	1	1	1	0	3	0	1	1	6	72	184
139	1	1	0	1	0	0	0	1	1	0	1	1	1	0	1	1	1	1	0	3	1	0	1	5	64	207
140	0	0	1	1	0	0	0	1	0	0	1	1	1	0	1	1	1	1	0	3	0	0	1	4	56	237
141	1	0	1	1	0	0	0	1	0	1	0	0	0	1	1	1	0	0	1	4	0	1	0	2	48	276
142	0	1	1	1	0	0	0	1	1	1	1	0	1	0	1	1	0	1	0	2	1	1	1	7	40	331
143	1	1	1	1	0	0	0	1	0	1	1	0	1	0	1	1	0	1	0	2	0	1	1	6	36	368
144	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	0	1	0	2	1	0	1	5	32	414
145	1	0	0	0	1	0	0	1	0	0	1	0	1	0	1	1	0	1	0	2	0	0	1	4	28	473
146	0	1	0	0	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
147	1	1	0	0	1	0	0	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
148	0	0	1	0	1	0	0	1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	1	7	20	663
149	1	0	1	0	1	0	0	1	0	1	1	1	0	0	1	1	1	0	0	1	0	1	1	6	18	736
150	0	1	1	0	1	0	0	1	1	0	1	1	0	0	1	1	1	0	0	1	1	0	1	5	16	828
151	1	1	1	0	1	0	0	1	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1	4	14	946
152	0	0	0	1	1	0	0	1	0	1	0	0	1	0	1	1	0	1	0	2	0	1	0	2	12	1104
153	1	0	0	1	1	0	0	1	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	10	1325
154	0	1	0	1	1	0	0	1	1	0	0	1	1	0	1	1	1	1	0	3	1	0	0	1	8	1656
155	1	1	0	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
156	0	0	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
157	1	0	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
158	0	1	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
159	1	1	1	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208

Table 7. PROM U25, Frequency — Fine 10-Hz Tuning.

DECIMAL INPUT	PROM U25																	U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS									IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																			
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8		A	B	C		A	B	C			
160	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1		1	1	1	7	0	0	0	0	NONE	0
161	1	0	0	0	0	1	0	1	1	1	1	1	1	1	0	1		1	1	1	7	1	1	1	7	2560	5
162	0	1	0	0	0	1	0	1	1	1	1	0	1	1	0	1		0	1	1	6	1	1	1	7	640	21
163	1	1	0	0	0	1	0	1	1	1	1	1	0	1	0	1		1	0	1	5	1	1	1	7	320	41
164	0	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1		1	0	1	5	0	0	1	4	224	59
165	1	0	1	0	0	1	0	1	1	1	1	0	0	1	0	1		0	0	1	4	1	1	1	7	160	83
166	0	1	1	0	0	1	0	1	1	0	1	0	0	1	0	1		0	0	1	4	1	0	1	5	128	104
167	1	1	1	0	0	1	0	1	0	0	1	0	0	1	0	1		0	0	1	4	0	0	1	4	112	118
168	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1		1	0	1	5	0	1	0	2	96	138
169	1	0	0	1	0	1	0	1	1	1	1	1	1	0	0	1		1	1	0	3	1	1	1	7	80	166
170	0	1	0	1	0	1	0	1	0	1	1	1	1	0	0	1		1	1	0	3	0	1	1	6	72	184
171	1	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1		1	1	0	3	1	0	1	5	64	207
172	0	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1		1	1	0	3	0	0	1	4	56	237
173	1	0	1	1	0	1	0	1	0	1	0	0	0	1	0	1		0	0	1	4	0	1	0	2	48	276
174	0	1	1	1	0	1	0	1	1	1	1	0	1	0	0	1		0	1	0	2	1	1	1	7	40	331
175	1	1	1	1	0	1	0	1	0	1	1	0	1	0	0	1		0	1	0	2	0	1	1	6	36	368
176	0	0	0	0	1	1	0	1	1	0	1	0	1	0	0	1		0	1	0	2	1	0	1	5	32	414
177	1	0	0	0	1	1	0	1	0	0	1	0	1	0	0	1		0	1	0	2	0	0	1	4	28	473
178	0	1	0	0	1	1	0	1	0	1	0	1	1	0	0	1		1	1	0	3	0	1	0	2	24	552
179	1	1	0	0	1	1	0	1	0	1	0	1	1	0	0	1		1	1	0	3	0	1	0	2	24	552
180	0	0	1	0	1	1	0	1	1	1	1	1	0	0	0	1		1	0	0	1	1	1	1	7	20	663
181	1	0	1	0	1	1	0	1	0	1	1	1	0	0	0	1		1	0	0	1	0	1	1	6	18	736
182	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	1		1	0	0	1	1	0	1	5	16	828
183	1	1	1	0	1	1	0	1	0	0	1	1	0	0	0	1		1	0	0	1	0	0	1	4	14	946
184	0	0	0	1	1	1	0	1	0	1	0	0	1	0	0	1		0	1	0	2	0	1	0	2	12	1104
185	1	0	0	1	1	1	0	1	1	1	0	1	0	0	0	1		1	0	0	1	1	1	0	3	10	1325
186	0	1	0	1	1	1	0	1	1	1	1	1	1	0	0	0		1	1	0	3	1	1	1	7	80	166
187	1	1	0	1	1	1	0	1	1	0	1	1	1	0	0	0		1	1	0	3	1	0	1	5	64	207
188	0	0	1	1	1	1	0	1	0	1	0	0	0	1	0	0		0	0	1	4	0	1	0	2	48	276
189	1	0	1	1	1	1	0	1	1	1	1	0	1	0	0	0		0	1	0	2	1	1	1	7	40	331
190	0	1	1	1	1	1	0	1	0	1	1	0	1	0	0	0		0	1	0	2	0	1	1	6	36	368
191	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0	0		0	1	0	2	1	0	1	5	32	414

Table 8. PROM U25, Frequency — Coarse 100-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
192	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	1	7	0	0	0	0	NONE	0
193	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	7	1	1	1	7	2560	5
194	0	1	0	0	0	0	1	1	1	1	1	0	1	1	1	1	0	1	1	6	1	1	1	7	640	21
195	1	1	0	0	0	0	1	1	1	1	1	1	0	1	1	1	1	0	1	5	1	1	1	7	320	41
196	0	0	1	0	0	0	1	1	0	0	1	1	0	1	1	1	1	0	1	5	0	0	1	4	224	59
197	1	0	1	0	0	0	1	1	1	1	1	0	0	1	1	1	0	0	1	4	1	1	1	7	160	83
198	0	1	1	0	0	0	1	1	1	0	1	0	0	1	1	1	0	0	1	4	1	0	1	5	128	104
199	1	1	1	0	0	0	1	1	0	0	1	0	0	1	1	1	0	0	1	4	0	0	1	4	112	118
200	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1	1	0	1	5	0	1	0	2	96	138
201	1	0	0	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	0	3	1	1	1	7	80	166
202	0	1	0	1	0	0	1	1	0	1	1	1	1	0	1	1	1	1	0	3	0	1	1	6	72	184
203	1	1	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	3	1	0	1	5	64	207
204	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	1	1	1	0	3	0	0	1	4	56	237
205	1	0	1	1	0	0	1	1	0	1	0	0	0	1	1	1	0	0	1	4	0	1	0	2	48	276
206	0	1	1	1	0	0	1	1	1	1	1	0	1	0	1	1	0	1	0	2	1	1	1	7	40	331
207	1	1	1	1	0	0	1	1	0	1	1	0	1	0	1	1	0	1	0	2	0	1	1	6	36	368
208	0	0	0	0	1	0	1	1	1	0	1	0	1	0	1	1	0	1	0	2	1	0	1	5	32	414
209	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	0	1	0	2	0	0	1	4	28	473
210	0	1	0	0	1	0	1	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
211	1	1	0	0	1	0	1	1	0	1	0	1	1	0	1	1	1	1	0	3	0	1	0	2	24	552
212	0	0	1	0	1	0	1	1	1	1	1	1	0	0	1	1	1	0	0	1	1	1	1	7	20	663
213	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1	1	1	0	0	1	0	1	1	6	18	736
214	0	1	1	0	1	0	1	1	1	0	1	1	0	0	1	1	1	0	0	1	1	0	1	5	16	828
215	1	1	1	0	1	0	1	1	0	0	1	1	0	0	1	1	1	0	0	1	0	0	1	4	14	946
216	0	0	0	1	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0	2	0	1	0	2	12	1104
217	1	0	0	1	1	0	1	1	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	3	10	1325
218	0	1	0	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	0	3	1	0	0	1	8	1656
219	1	1	0	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
220	0	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
221	1	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
222	0	1	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208
223	1	1	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	2	6	2208

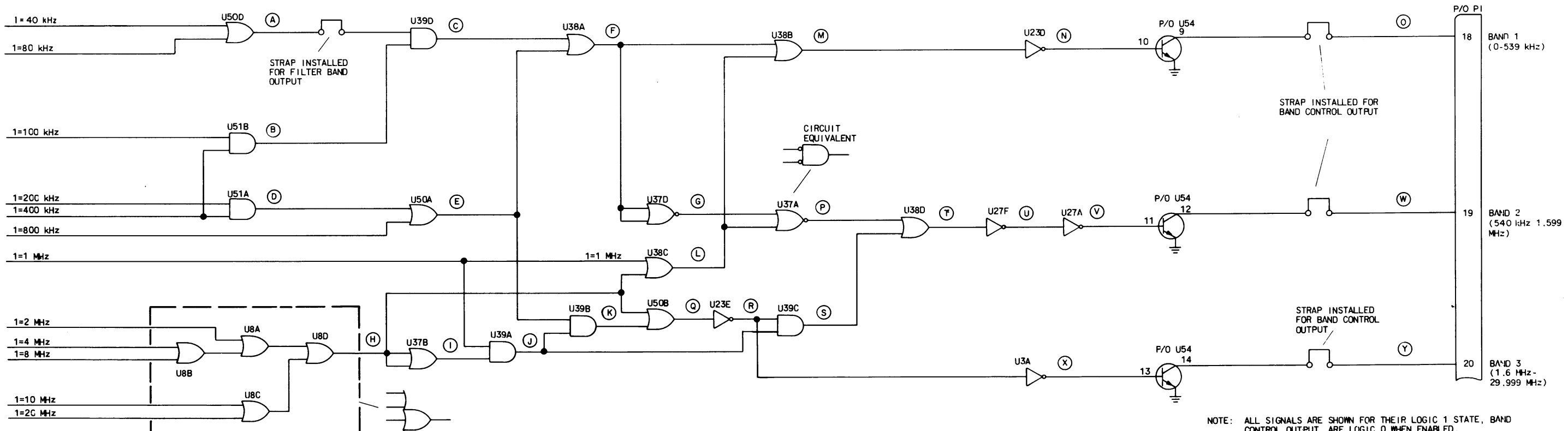
Table 9. PROM U25, Frequency — Fine 100-Hz Tuning.

DECIMAL INPUT	PROM U25																U7				U24				DIVISION RATIO	APPROX VARIABLE CLOCK FREQ (Hz)
	RATE					FINE TUNE	VBFO		OUTPUTS								IN			OUT CH	IN			OUT CH		
	1	2	4	8	16		10 Hz	1 Hz																		
	0	1	2	3	4	5	6	7	1	2	3	4	5	6	7	8	A	B	C		A	B	C			
224	0	0	0	0	0	1	1	1	0	0	0	1	1	1	0	0	1	1	1	7	0	0	0	0	NONE	0
225	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1	1	1	7	1	1	1	7	2560	5
226	0	1	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	1	1	6	1	1	1	7	640	21
227	1	1	0	0	0	1	1	1	1	1	1	1	0	1	0	0	1	0	1	5	1	1	1	7	320	41
228	0	0	1	0	0	1	1	1	0	0	1	1	0	1	0	0	1	0	1	5	0	0	1	4	224	59
229	1	0	1	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	1	4	1	1	1	7	160	83
230	0	1	1	0	0	1	1	1	1	0	1	0	0	1	0	0	0	0	1	4	1	0	1	5	128	104
231	1	1	1	0	0	1	1	1	0	0	1	0	0	1	0	0	0	0	1	4	0	0	1	4	112	118
232	0	0	0	1	0	1	1	1	0	1	0	1	0	1	0	0	1	0	1	5	0	1	0	2	96	138
233	1	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	1	1	0	3	1	1	1	7	80	166
234	0	1	0	1	0	1	1	1	0	1	1	1	1	0	0	0	1	1	0	3	0	1	1	6	72	184
235	1	1	0	1	0	1	1	1	1	0	1	1	1	0	0	0	1	1	0	3	1	0	1	5	64	207
236	0	0	1	1	0	1	1	1	0	0	1	1	1	0	0	0	1	1	0	3	0	0	1	4	56	237
237	1	0	1	1	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1	4	0	1	0	2	48	276
238	0	1	1	1	0	1	1	1	0	1	0	0	0	1	0	0	0	0	1	4	0	1	0	2	48	276
239	1	1	1	1	0	1	1	1	1	1	1	0	1	0	0	0	0	1	0	2	1	1	1	7	40	331
240	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	1	0	2	1	1	1	7	40	331
241	1	0	0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1	0	2	0	1	1	6	36	368
242	0	1	0	0	1	1	1	1	0	1	1	0	1	0	0	0	0	1	0	2	0	1	1	6	36	368
243	1	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0	0	1	0	2	1	0	1	5	32	414
244	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0	2	0	0	1	4	28	473
245	1	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0	2	0	0	1	4	28	473
246	0	1	1	0	1	1	1	1	0	1	0	1	1	0	0	0	1	1	0	3	0	1	0	2	24	552
247	1	1	1	0	1	1	1	1	0	1	0	1	1	0	0	0	1	1	0	3	0	1	0	2	24	552
248	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	1	7	20	663
249	1	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	1	7	20	663
250	0	1	0	1	1	1	1	1	0	1	1	1	0	0	0	0	1	0	0	1	0	1	1	6	18	736
251	1	1	0	1	1	1	1	1	1	0	1	1	0	0	0	0	1	0	0	1	1	0	1	5	16	828
252	0	0	1	1	1	1	1	1	1	0	1	1	0	0	0	0	1	0	0	1	1	0	1	5	16	828
253	1	0	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	4	14	946
254	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	4	14	946
255	1	1	1	1	1	1	1	1	0	1	0	0	1	0	0	0	0	1	0	2	0	1	0	2	12	1104

2.4.2 1/2-Octave Control Output Circuits

(Refer to figure 4.)

When strapped for 1/2-octave filter control (OF), the 1/2-octave control output circuits receive parallel bcd input control signals (from storage registers U29-U36) and convert them to one-of-eleven 1/2-octave control output signals. Frequency ranges of the bands and PROM U10 decoding are shown in table 10.



NOTE: ALL SIGNALS ARE SHOWN FOR THEIR LOGIC 1 STATE, BAND CONTROL OUTPUT ARE LOGIC 0 WHEN ENABLED.

CIRCUIT EQUIVALENT

	BCD LOGIC FORMULA	FREQUENCY RANGE
(A)	$40 + 80$	=40 THROUGH 99 kHz
(B)	$100 \cdot 400$	=500 THROUGH 599 kHz
(C)	$[40 + 80]\ [100 \cdot 400]$	=540 THROUGH 599 kHz
(D)	$200 \cdot 400$	=600 THROUGH 799 kHz
(E)	$(200 \cdot 400) + 800$	=600 THROUGH 999 kHz
(F)	$([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800$	=540 THROUGH 999 kHz
(G)	$\overline{([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800}$	=$\overline{540 \text{ THROUGH } 999 \text{ kHz}}$
(H)	$2 + 4 + 8 + 10 + 20$	=2 THROUGH 29.999 MHz
(I)	$\overline{2 + 4 + 8 + 10 + 20}$	=$\overline{2 \text{ THROUGH } 29.999 \text{ MHz}}$
(J)	$1 \cdot (\overline{2 + 4 + 8 + 10 + 20})$	=1 THROUGH 1.999 MHz
(K)	$[(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]$	=1.600 THROUGH 1.999 MHz
(L)	$1 + 2 + 4 + 8 + 10 + 20$	=1 THROUGH 29.999 MHz

	BCD LOGIC FORMULA	FREQUENCY RANGE
(M)	$([40 + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20$	=540 kHz THROUGH 29.999 MHz
(N)	$\overline{([40 + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20}$	=$\overline{540 \text{ kHz THROUGH } 29.999 \text{ MHz}}$
(O)	SAME AS (M)	=$\overline{0 \text{ THROUGH } 539 \text{ kHz}}$ (BAND 1)
(P)	$[([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800] \cdot \overline{(1 + 2 + 4 + 8 + 10 + 20)}$	=540 THROUGH 999 kHz
(Q)	$([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20$	=1.600 THROUGH 29.999 MHz
(R)	$\overline{([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})])} + 2 + 4 + 8 + 10 + 20$	=$\overline{1.600 \text{ THROUGH } 29.999 \text{ MHz}}$
(S)	$[1 \cdot (\overline{2 + 4 + 8 + 10 + 20})] \cdot \overline{[([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20]}$	=1.000 THROUGH 1.599 MHz
(T)	$([([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800] \cdot \overline{[1 + 2 + 4 + 8 + 10 + 20]}) +$ $([1 \cdot (\overline{2 + 4 + 8 + 10 + 20})] \cdot \overline{[([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20]})$	= 540 kHz THROUGH 1.599 MHz
(U)	$\overline{([([40 + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) \cdot 800] \cdot \overline{[1 + 2 + 4 + 8 + 10 + 20]}) +}$ $\overline{([1 \cdot (\overline{2 + 4 + 8 + 10 + 20})] \cdot [([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20])}$	=$\overline{540 \text{ kHz THROUGH } 1.599 \text{ MHz}}$
(V)	SAME AS (T)	=540 kHz THROUGH 1.599 MHz
(W)	SAME AS (U)	=$\overline{540 \text{ kHz THROUGH } 1.599 \text{ MHz}}$ (BAND 2)
(X)	$([(200 \cdot 400) + 800] \cdot [1 \cdot (\overline{2 + 4 + 8 + 10 + 20})]) + 2 + 4 + 8 + 10 + 20$	=1.600 THROUGH 29.999 MHz
(Y)	SAME AS (R)	=$\overline{1.600 \text{ THROUGH } 29.999 \text{ MHz}}$ (BAND 3)

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Band Control Output Circuits
Figure 3

Table 10. PROM U10, 1/2-Octave Control.

BAND	BAND FREQ RANGE (MHz)	HEXADECIMAL INPUTS	HEXADECIMAL INPUTS								OUTPUTS							
			1	2	4	8	10	20	40	80	1	2	3	4	5	6	7	8
			ADDRESS INPUTS															
			0	1	2	3	4	5	6	7								
*1	0-0.559	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
*2	0.560-1.599	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
*3	1.600-1.999	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	2.000-2.999	2	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
5	3.000-3.999	3	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
6	4.000-5.999	4	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
		5	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
7	6.000-7.999	6	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
		7	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0
8	8.000-11.999	8	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
		9	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
		10	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
		11	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
9	12.000-15.999	12	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
		13	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0
		14	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0
		15	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0
10	16.000-23.999	16	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0
		17	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0
		18	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0
		19	1	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0
		20	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
		21	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
		22	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
		23	1	1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
11	24.000-29.999	24	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		25	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		26	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		27	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1
		28	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1
		29	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1

*Bands 1, 2, and 3 not selected by PROM.

Refer to figure 4 and table 10 and note that any bcd frequency that lies between the low frequency of one band and the low frequency of the next higher band provides the associated 1/2-octave control output signal (logic 1 = enabled).

2.5 Fault and Monitor Circuits (Refer to figure 5.)

The following fault and monitor circuits are included in this control card:

a. Receiver fault signal (logic 1 = fault) is generated by a power supply fault (logic 1), a vbfo synthesizer fault (logic 1), or a synthesizer fault (logic 1). A power-on (restored) condition or a power supply fault input causes the receiver fault to be latched in the fault mode. The power supply fault is cleared by changing frequency. The synthesizer and vbfo synthesizer faults are cleared when the fault is removed.
b. Receive rf overload indication (logic 1 = overload) is generated by a preselector rf overload (logic 1) or a receive rf overload (logic 1) input. The +5 V dc connected through the diode in the preselector rf overload input line is a high-level protector that prevents any signal in excess of +5 V dc from being applied to NOR gate U37C.
c. Preselector fault indication (logic 1 = fault) is generated by a preselector fault (logic 1) input. The +5 V dc connected through the diode in the preselector fault input line is a high-level protector that prevents any signal in excess of +5 V dc from being applied to buffer/driver U3C.
d. 450-kHz enable (logic 1 = enable) is generated by an SSB mode (logic 1) input.

2.6 Tune Start Circuit (Refer to figure 6.)

The tune start pulse (ground pulse at P1-99) is initiated by making an operating frequency change and/or a change in local-remote status.

Tune start pulser U15A is a retriggerable, monostable multivibrator and holds P1-99 (through Q14) at ground as long as input U15A-4 is constantly changing. Tune start pulse width is a function of R32, C2, and the frequency of triggers applied at U15A-4.

When a local enable signal is initially applied, a tune start pulse is supplied at P1-99. The same is true when the local enable signal is initially removed.

When a local enable signal is not applied (logic 0 applied), $\overline{\text{clock inhibit}}$ is applied (logic 1), and a remote frequency change signal is applied; U16C is NANDed and supplies a logic 0 to U18C where it is ANDed and supplies a logic 1 to U15B-12. The logic 1 at U15B-12 causes a single pulse output. The pulse from U15B is applied to U15A-5 which supplies a tune start pulse output at P1-99.

When $\overline{\text{clock inhibit}}$ is applied (logic 1) and vbfo tune is not applied (logic 0 applied), a change of the front-panel tune control produces a local frequency change. The movement of the front-panel tune control causes the variable clock to be applied to U11A-1. The variable clock is ANDed by U11A, applied to and ANDed by U11B, and supplied as clock pulses through U13D to U15A-4. U15A produces a tune start pulse whose duration is controlled by R32, C2, and the continuous application of variable clock pulses (these continue to be applied until turning of the knob is stopped).

When $\overline{\text{clock inhibit}}$ is logic 0, U2C output is logic 1 and U2B output is logic 0 inhibiting U16C, U18C, and U15B. The logic 0 from U2B also inhibits U11B.

2.7 VBFO Tune Circuit (Refer to figure 6.)

When vbfo tune is logic 1, U17F output is logic 0 and U11A output is logic 0 inhibiting U11B. With vbfo at logic 1 and $\overline{\text{clock inhibit}}$ at logic 1, U11D and U11C are enabled and variable clock pulses applied at U11D-13 are supplied as vbfo clock pulses out at P1-85.

When vbfo tune is logic 1, a logic 1 output is supplied as WD1G at P1-69, and with no WD4 strobe applied a logic 0 output is supplied as WD3G at P1-68.

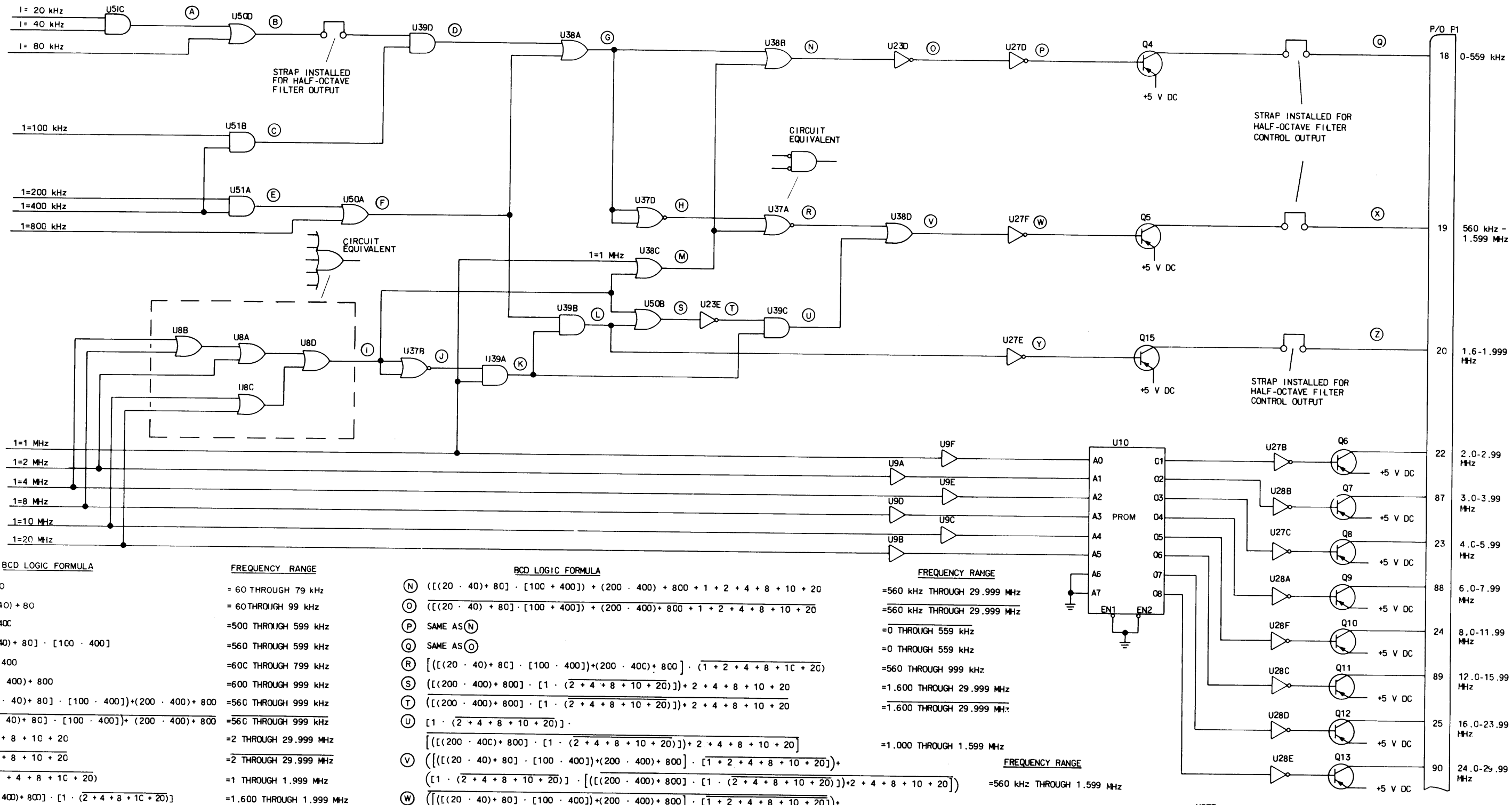
3. TESTING/TROUBLESHOOTING PROCEDURES

3.1 Test Equipment and Power Requirements

Test equipment and power sources required to test, troubleshoot, and repair the control card are listed in the maintenance section of this instruction book.

3.2 Testing

The test procedures in table 11 check total performance of the control card. These test procedures permit isolation of a fault to a specific component or circuit when the results are used with the schematic to circuit trace the fault.



BCD LOGIC FORMULA	FREQUENCY RANGE
(A) $20 \cdot 40$	= 60 THROUGH 79 kHz
(B) $(20 \cdot 40) + 80$	= 60 THROUGH 99 kHz
(C) $100 \cdot 400$	=500 THROUGH 599 kHz
(D) $[(20 \cdot 40) + 80] \cdot [100 \cdot 400]$	=560 THROUGH 599 kHz
(E) $200 \cdot 400$	=600 THROUGH 799 kHz
(F) $(200 \cdot 400) + 800$	=600 THROUGH 999 kHz
(G) $([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800$	=560 THROUGH 999 kHz
(H) $\overline{[20 \cdot 40) + 80] \cdot [100 \cdot 400])} + (200 \cdot 400) + 800$	=560 THROUGH 999 kHz
(I) $2 + 4 + 8 + 10 + 20$	=2 THROUGH 29.999 MHz
(J) $\overline{2 + 4 + 8 + 10 + 20}$	=2 THROUGH 29.999 MHz
(K) $1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}$	=1 THROUGH 1.999 MHz
(L) $[(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]$	=1.600 THROUGH 1.999 MHz
(M) $1 + 2 + 4 + 8 + 10 + 20$	=1 THROUGH 29.999 MHz

BCD LOGIC FORMULA	FREQUENCY RANGE
(N) $([(20 \cdot 40) + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20$	=560 kHz THROUGH 29.999 MHz
(O) $\overline{([(20 \cdot 40) + 80] \cdot [100 + 400]) + (200 \cdot 400) + 800 + 1 + 2 + 4 + 8 + 10 + 20}$	=560 kHz THROUGH 29.999 MHz
(P) SAME AS (N)	=0 THROUGH 559 kHz
(Q) SAME AS (O)	=0 THROUGH 559 kHz
(R) $\left[([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800\right] \cdot \overline{(1 + 2 + 4 + 8 + 10 + 20)}$	=560 THROUGH 999 kHz
(S) $([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20$	=1.600 THROUGH 29.999 MHz
(T) $\overline{([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20}$	=1.600 THROUGH 29.999 MHz
(U) $[1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}] \cdot \overline{\left[([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20\right]}$	=1.000 THROUGH 1.599 MHz
(V) $\left(\left[([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800\right] \cdot \overline{[1 + 2 + 4 + 8 + 10 + 20]}\right) + \left(\overline{[1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]} \cdot \left[([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20\right]\right)$	=560 kHz THROUGH 1.599 MHz
(W) $\left(\overline{\left[([(20 \cdot 40) + 80] \cdot [100 \cdot 400]) + (200 \cdot 400) + 800\right] \cdot [1 + 2 + 4 + 8 + 10 + 20]}\right) + \left(\overline{[1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]} \cdot \left[([(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]) + 2 + 4 + 8 + 10 + 20\right]\right)$	=560 kHz THROUGH 1.599 MHz
(X) SAME AS (V)	=560 kHz THROUGH 1.599 MHz
(Y) $\overline{[(200 \cdot 400) + 800] \cdot [1 \cdot \overline{(2 + 4 + 8 + 10 + 20)}]}$	=1.600 THROUGH 1.999 MHz
(Z) SAME AS (L)	=1.600 THROUGH 1.999 MHz

NOTE

(1) ALL SIGNALS ARE SHOWN FOR THEIR LOGIC 1 STATE, HALF-OCTAVE FILTER CONTROL OUTPUTS ARE LOGIC 1 WHEN ENABLED.

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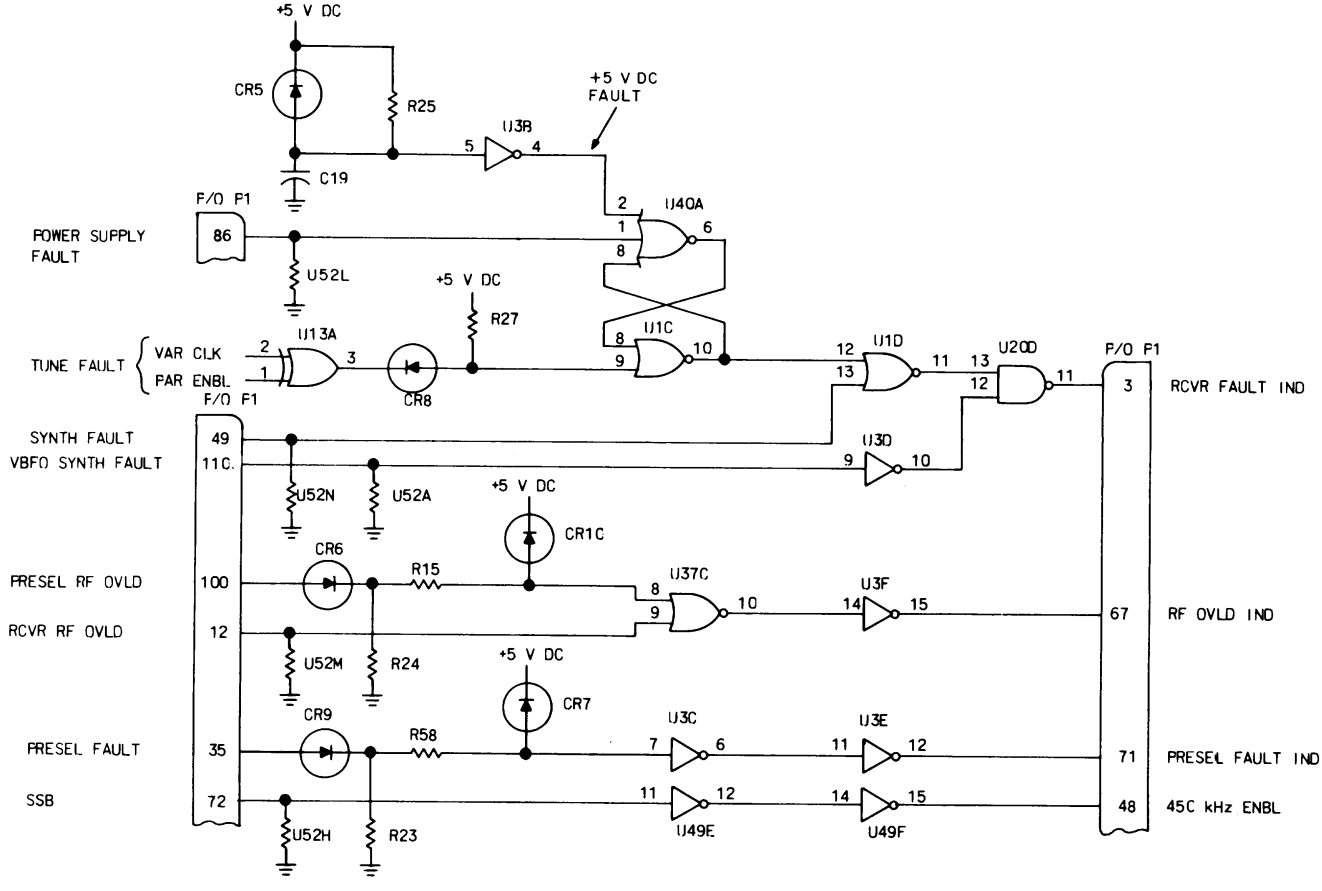
1/2-Octave Filter Control Output Circuits
Figure 4



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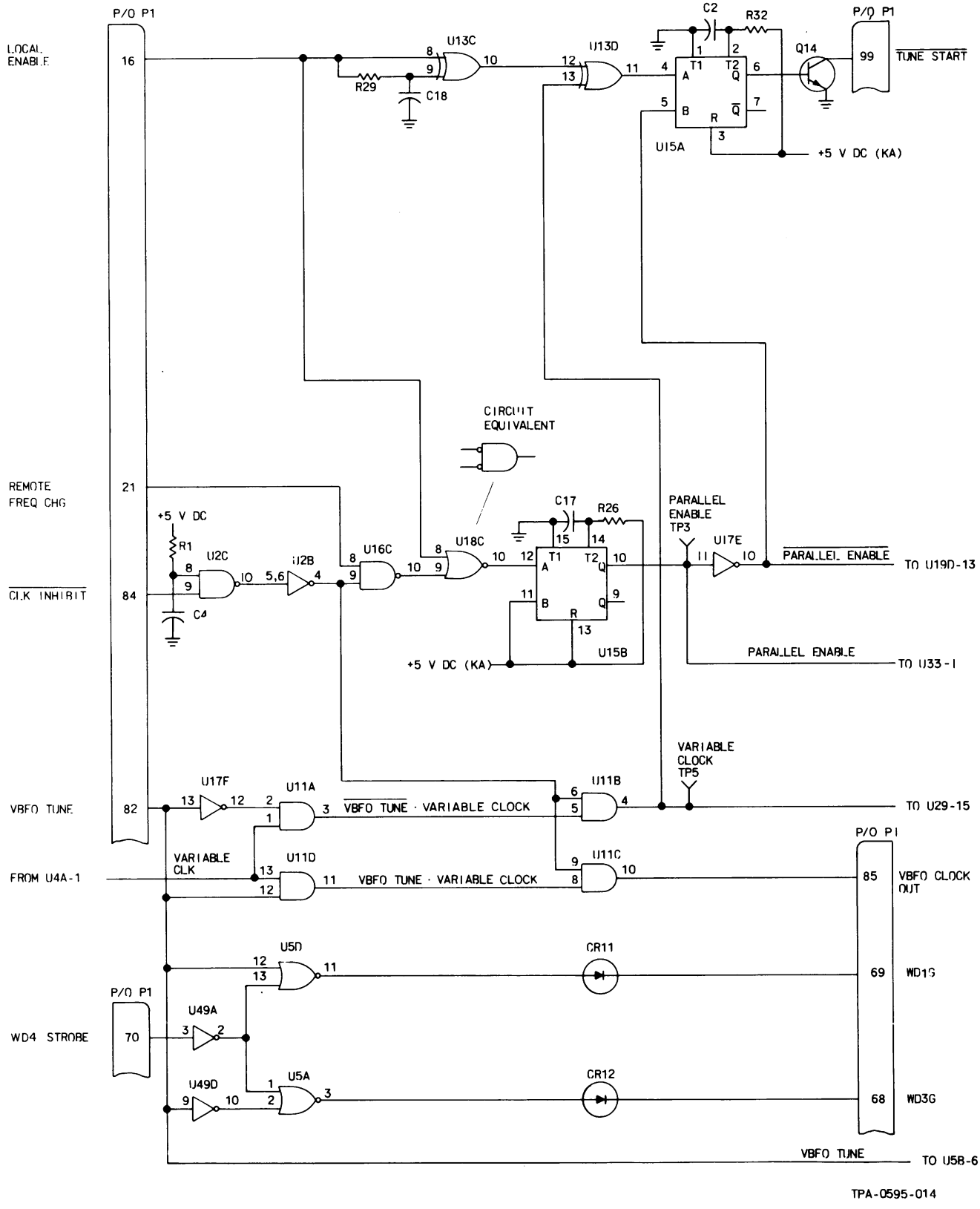
Control and Fault Indications
Figure 5



Tune Start and Vbfo Control
Figure 6

Table 11. Control, Testing and Troubleshooting Procedures.

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
1. Setup	a. Remove top cover of unit containing the control that is to be tested. b. If installed, remove parallel input, parallel output, and serial interface. Note If removed, upon completion of control testing, reinstall parallel input, parallel output, and serial interface. c. Remove control. Install it on extender and place it in the unit. d. Set unit LINE SELECTOR for power source available (100/115/215/230 V ac). Note Ensure that proper fuse is installed for power source used. e. Connect unit to available power source. Caution In the following procedures, when applying +5-V dc or 0-V dc (ground) to the indicated points, apply these levels through a 100-ohm or more series limiting resistor. The +5-V dc source should be obtained from the receiver power supply so that the integrated circuit supply voltages are not exceeded by the applied levels.		
2. Initial outputs (Cont)	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
2. (Cont)	b. Measure dc voltages between the following pins and ground (TP1, brown):		Check associated power supply.
	P1-45 P1-65 P1-114	+15 ±1.0 V dc +5 ±0.5 V dc -15 ±1.0 V dc	
	c. Note front-panel indications.	FREQUENCY·KHZ is 00 000.000 (Refer to test 9 for logic levels at 00 000.000). Note Because of keep-alive feature, previously stored FREQUENCY KHZ may be in memory.	Check U29 through U36, and variable clock circuit.
		RCV FAULT is lit. (logic 1 at P1-3).	Check U15B, U18C, U16C, and variable clock circuits.
	d. Check dc voltage at TP4 (3-state control).	NMT 0.5 V dc.	Check U19B, U19C, U17C, U2B, U2C, and associated circuits.
	e. Check dc voltage at TP5 (variable clock).	NMT 0.5 V dc.	Check U11B and associated circuits.
3. 3-State buffer control	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply a ground to P1-113 (parallel frequency enable).		
	c. Measure dc voltage at TP 4.	NMT 0.5 V dc.	Check U19C and associated circuit.
	d. Apply a ground to P1-84 ($\overline{\text{clock inhibit}}$).		
(Cont)	e. Measure dc voltage at TP4.	NLT +3.0 V dc.	Check U2C, U2B, U19B, and associated circuit.

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
3. (Cont)	f. Remove P1-84 and P1-113 grounds.		
	g. Connect +5 V dc to P1-113.		
	h. Measure dc voltage at TP4.	NMT 0.5 V dc.	Check U19B and associated circuit.
	i. Set CONT to REM (removes +5 V dc from P1-16, local enable).		
	j. Measure dc voltage at TP4.	NLT +3.0 V dc.	Same as step 3.h.
	k. Remove +5 V dc from P1-113.		
4. Receiver fault latch	a. Connect an oscilloscope to P1-99 (tune start).		
	b. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	c. Apply momentary +5 V dc to P1-21 (remote frequency change).	Note that a tune start pulse is generated (displayed on oscilloscope).	Check U16C, U18C, U15, U17E, Q14, and associated circuit.
	d. Measure dc voltage at P1-3 (receiver fault indication).	NMT 0.5 V dc (RCV FAULT indicator goes out).	Check U16C, U18C, U15B, U13A, U1C, and associated circuit.
	e. Set CONT to LCL (applies +5 V dc to P1-16, local enable).		
	f. Apply a momentary +5 V dc to P1-86 (power supply fault).		
	g. Measure dc voltage at P1-3.	NLT +3.0 V dc (RCV FAULT indicator lights).	Check U40A, U1C, U1D, U20D, and associated circuit.
	h. Apply +5 V dc to P1-30 (rate (1)).		
	i. Measure dc voltage at P1-3.	NMT 0.5 V dc (RCV FAULT indicator goes out).	Check U11B, U13A, U1C, and associated circuit.
(Cont)	j. Remove +5 V dc from P1-30.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
4. (Cont)	k. Measure dc voltage at P1-3.	NMT 0.5 V dc (RCV FAULT indicator remains out).	Same as step 4.i.
	l. Apply momentary +5 V dc to P1-86.		
	m. Measure dc voltage at P1-3.	NLT +3.0 V dc (RCV FAULT indicator lights).	Same as step 4.g.
	n. Apply momentary +5 V dc to P1-21 (several times).		
	o. Measure dc voltage at P1-3.	NLT +3.0 V dc (RCV FAULT indicator remains lit).	Check U18C and associated circuits.
	p. Apply a momentary +5 V dc to P1-30.		
5. Word 4 strobe routing	a. Front-panel controls set as follows: PWR to on. CONT to any. MODE to SSB/CW. BANDWIDTH to 16. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply +5 V dc to P1-70 (word 4 strobe).		
	c. Measure dc voltage at P1-69 (WDIG).	NLT +3.0 V dc.	Check U49A, U5D, and associated circuit.
	d. Measure dc voltage at P1-68 (WD3G).	NMT 0.5 V dc.	Check U49A, U5A, and associated circuit.
	e. Set BFO switch to TUNE (applies +5 V dc to P1-82, vbfo tune).		
	f. Measure dc voltage at P1-69.	NMT 0.5 V dc.	Same as step 5c.
	g. Measure dc voltage at P1-68.	NLT +3.0 V dc.	Same as step 5d.
	h. Remove +5 V dc from P1-70 and set BFO switch to FIX (removes +5 V dc from P1-82).		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
6. Tune start	a. Connect an oscilloscope to P1-99 (tune start).		
	b. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to SSB/CW. BANDWIDTH to 16. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	c. Set CONT switch to LCL (applied +5 V dc to P1-16.	Note that a tune start pulse is generated (displayed on oscilloscope) when CONT switch is just switched to LCL.	Check U13C, U13D, U15A, Q14, and associated circuits.
	d. Set CONT switch to REM (removes +5 V dc from P1-16).	Note that a tune start pulse is generated when CONT switch is just switched to REM.	Same as step 6.a.
7. Counter parallel enable	a. Connect an oscilloscope to TP3 (parallel enable).		
	b. Front-panel controls set as follows: PWR to on. CONT to REM. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		Check U16C, U18C, U15B and associated circuits.
	c. Apply a momentary +5 V dc to P1-21 (remote frequency change).	Note that a logic 1 parallel enable pulse is generated 0.5 to 2.5 ms long.	
	d. Repeat as often as necessary to obtain accurate pulse length.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
8. Fault and interface circuits	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to any. BANDWIDTH to any. DIAL to LOCK. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Apply +5 V dc at P1-49 (synthesizer fault).		
	c. Measure dc voltage at P1-3 (receiver fault indication).	NLT +3.0 V dc (RCV FAULT indicator lights).	Check U1D, U20D, and associated circuits.
	d. Remove +5 V dc from P1-49.		
	e. Apply +5 V dc at P1-110 (vbfo synthesizer fault).		
	f. Measure dc voltage at P1-3 (receiver fault indication).	NLT +3.0 V dc (RCV FAULT indicator lights).	Check U3D, U20D, and associated circuits.
	g. Remove +5 V dc from P1-110.		
	h. Apply +5 V dc at P1-35 (preselector fault).		
	i. Measure dc voltage at P1-71 (preselector fault indication).	NLT +3.0 V dc (PRESEL FAULT indicator lights).	Check U3C, U3E, and associated circuits.
	j. Remove +5 V dc from P1-35.		
	k. Apply +5 V dc at P1-100 (preselector rf overload).		
	l. Measure dc voltage at P1-67 (rf overload indication).	NLT +3.0 V dc (RCV OVERLOAD indicator lights).	Check U37C, U3F, and associated circuits.
	m. Remove +5 V dc from P1-100.		
	n. Set MODE switch to SSB/CW (applies +5 V dc to P1-72, ssb enable).		
	o. Measure dc voltage at P1-48 (450-kHz enable).	NLT +3.0 V dc.	Check U49E, U49F, and associated circuits.
	p. Set MODE switch to AM (removes +5 V dc from P1-72).		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

<table>
<tr><th>TEST</th><th>PROCEDURE</th><th>NORMAL INDICATION</th><th>IF INDICATION IS ABNORMAL</th></tr>
<tr><td>9. Parallel frequency control

(Cont)</td><td>a. Front-panel controls set as follows:

PWR to on.
CONT to REM.
MODE to SSB/CW.
BANDWIDTH to USB.
DIAL to LOCK.
BFO to FIX.
AGC to FAST.
RF GAIN to full cw.

b. Apply +5 V dc to P1-113 (parallel frequency enable).

c. Refer to chart below to apply any parallel bcd frequency input to P1.

d. With any noted bcd frequency input applied, momentarily apply +5 V dc to P1-Z1 (remote frequency change).

e. Remove +5 V dc from P1-113.

f. Remove applied bcd frequency input and measure dc voltages at all bcd input pins.

g. Repeat steps c, d, e, and f at several different frequency inputs.</td><td>Should be same as noted frequency input in step c. (Front-panel FREQUENCY KHZ indicators should indicate the applied bcd frequency input of step c.)</td><td>Check U29 thru U36, U42 thru U48, and associated circuits.</td></tr>
</table>

BCD WT	BCD INPUT PINS (Hz)								LOGIC INPUTS FOR EACH DIGIT									
	1	10	100	1k	10k	100k	1M	10M										
	CONNECTOR PIN P1-( )								0	1	2	3	4	5	6	7	8	9
1	50	52	54	56	58	60	62	64	0	1	0	1	0	1	0	1	0	1
2	115	117	119	121	123	125	127	129	0	0	1	1	0	0	1	1	0	0
4	51	53	55	57	59	61	63	-	0	0	0	0	1	1	1	1	0	0
8	116	118	120	122	124	126	128	-	0	0	0	0	0	0	0	0	1	1
Logic 1 = +3.0 to +5.5 V dc. Logic 0 = NMT 0.5 V dc (ground).																		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
9. (Cont)	h. Apply +5 V dc to P1-113 (parallel frequency enable). i. Apply bcd frequency input for 00 000.000 kHz. j. Momentarily apply +5 V dc to P1-21 (remote frequency change). k. Remove +5 V dc from P1-113. l. Remove bcd frequency input. m. Set CONT switch to LCL (applied +5 V dc to P1-16, local enable). n. Measure dc voltages at all bcd input pins. o. Repeat steps h thru m at each of the following frequencies: 11 111.111 22 222.222 23 333.333 24 444.444 25 555.555 26 666.666 27 777.777 28 888.888 29 999.999	Should be same as frequency applied. (Front-panel FREQUENCY KHZ indicators should indicate the applied bcd frequency input.)	Same as step 9.f.
10. Band decoder, 1/2-octave (applicable only with OF strapping) (Cont)	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw. b. Rotate TUNING knob thru the frequency range of the receiver. Note the exact frequency that each 1/2-octave band output changes (see table below).		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL

10. (Cont)

BAND	FREQUENCY RANGE (MHz)	LOGIC LEVELS P1-( )											CHECK
		18	19	20	22	87	23	88	24	89	25	90	
1	0.000-0.559	1	0	0	0	0	0	0	0	0	0	0	Q4
2	0.560-1.599	0	1	0	0	0	0	0	0	0	0	0	Q5
3	1.600-1.999	0	0	1	0	0	0	0	0	0	0	0	Q15
4	2.000-2.999	0	0	0	1	0	0	0	0	0	0	0	Q6
5	3.000-3.999	0	0	0	0	1	0	0	0	0	0	0	Q7
6	4.000-5.999	0	0	0	0	0	1	0	0	0	0	0	Q8
7	6.000-7.999	0	0	0	0	0	0	1	0	0	0	0	Q9
8	8.000-11.999	0	0	0	0	0	0	0	1	0	0	0	Q10
9	12.000-15.000	0	0	0	0	0	0	0	0	1	0	0	Q11
10	16.000-23.999	0	0	0	0	0	0	0	0	0	1	0	Q12
11	24.000-29.999	0	0	0	0	0	0	0	0	0	0	1	Q13

Logic 1 = +3.0 to 5.5-V dc (enable).
Logic 0 = NMT 0.5-V dc (disable).

11. Band decoder, standard (applicable only with SF strapping)

a. Front-panel controls set as follows:

PWR to on.
CONT to LCL.
MODE to SSB/CW.
BANDWIDTH to USB.
DIAL to FINE.
BFO to FIX.
AGC to FAST.
RF GAIN to full cw.

b. Rotate TUNING knob thru the frequency range of the receiver. Note the exact frequency that each standard band output changes. (See table that follows.)

BAND	FREQUENCY RANGE (MHz)	LOGIC LEVELS P1-( )			CHECK
		18	19	20	
1	0.000-0.539	0	1	1	U54, U23D
2	0.540-1.599	1	0	1	U54, U22A
3	1.600-29.999	1	1	0	U54, U23A

Logic 1 = open circuit (disable).
Logic 0 = ground (enable).

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. Clocked frequency counter, fine tune	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Rotate the TUNING knob slowly in a clockwise direction.		
	c. Observe front-panel FREQUENCY KHZ display.	The lowest order digit is clocked up and carries over to the next higher digit as the TUNING knob is rotated.	Check variable clock at TP5. If clock available, check U29 thru U36. If clock not available, check U25 and associated circuits. If direction wrong, check input at P1-27.
	d. Rotate the TUNING knob slowly in a counterclockwise direction.		
	e. Observe front-panel FREQUENCY KHZ display.	The lowest order digit is clocked down and borrows from the next higher digit as the TUNING knob is rotated.	Same as step c.
	f. Repeat step b at increased speed and rotate clockwise thru entire frequency range plus.		
(Cont)	g. Observe front-panel FREQUENCY KHZ display.	Same as step c. Note that when hundredths are clocked thru they carry over to tenths, when tenths are clocked thru they carry over to ones, etc. When 29 999.99 kHz is clocked thru it starts over at 000.00 kHz.	Same as step c.

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
12. (Cont)	h. Repeat step d at increased speed and rotate counterclockwise thru entire frequency range plus.		
	i. Observe front-panel FREQUENCY KHZ display.	Same as step e. Note that when hundredths are clocked thru they borrow from tenths, when tenths are clocked thru they borrow from ones, etc. When 000.00 kHz is clocked thru it starts over at 29 999.99 kHz.	Same as step c.
13. Clocked frequency counter, coarse tune	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to CRS. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Rotate the TUNING knob slowly in a clockwise direction.		
	c. Observe front-panel FREQUENCY KHZ display.	The 10-kHz digit is clocked up and carries over to the next higher digit as the TUNING knob is rotated.	Check U34 thru U36 and associated circuits.
	d. Rotate the TUNING knob slowly in a counterclockwise direction.		
	e. Observe front-panel FREQUENCY KHZ display.	The 10-kHz digit is clocked down and borrows from the next higher digit as the TUNING knob is rotated.	Same as step c.
(Cont)	f. Repeat step b at increased speed and rotate clockwise thru entire frequency range plus.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
13. (Cont)	g. Observe front-panel FREQUENCY KHZ display.	Same as step c. Note that when 10 kHz are clocked thru, they carry over to 100 kHz, when 100 kHz are clocked thru they carry over to 1 MHz, etc. When 29 990.00 kHz is clocked thru it starts over at 000.00 kHz.	Same as step c.
	h. Repeat step d at increased speed and rotate counterclockwise thru entire frequency range plus.		
	i. Observe front-panel FREQUENCY KHZ display.	Same as step e. Note that when 10 kHz are clocked thru they borrow from 100 kHz, when 100 kHz are clocked thru they borrow from 1 MHz, etc. When 000.00 kHz is clocked thru it starts over at 29 990.00 kHz.	Same as step c.
14. Clocked frequency counter, clock inhibit	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. While rotating the TUNING knob and observing the FREQUENCY KHZ display, apply ground to P1-84 (clock inhibit).	Frequency display is clocked until +5 V dc is applied at P1-84, when the clocking is ceased and the front-panel FREQUENCY KHZ displays 000.00.	Check U2C, U2B, U17F, U11A, U11B, and associated circuits. If 000.00 is not displayed check U42 thru U4B and associated circuits.
(Cont)	c. Stop rotating the TUNING knob.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
14. (Cont)	d. Remove ground from P1-84.		
	e. Observe FREQUENCY KHZ display.	Frequency last displayed, before +5 V dc was applied to P1-84, should be displayed.	Check U29 thru U36 and associated circuits.
15. Vbfo clock	a. Front-panel controls set as follows: PWR to on. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to TUNE. AGC to FAST. RF GAIN to full cw.		
	b. Rotate the TUNING knob slowly in a clockwise direction.		
	c. Observe front-panel VBFO OFFSET HZ display.	The tens-Hz digit is clocked up. (Note that carryover and up/down direction of the vbfo frequency is not a function of the control card).	Check U11D, U11C and associated circuits.
	d. Rotate the TUNING knob slowly in a counterclockwise direction.		
	e. Observe front-panel VBFO OFFSET HZ display.	The tens-Hz digit is clocked down.	Same as step c.
	f. Set DIAL switch to CRS.		
	g. Rotate the TUNING knob slowly in a clockwise direction.		
	h. Observe front-panel VBFO OFFSET HZ display.	The tens-Hz digit is clocked up at about the same speed as when the DIAL switch was set to FINE.	Check U25 and associated circuits.
	i. While rotating the TUNING knob and observing the VBFO OFFSET HZ display, apply ground to P1-84 (clock inhibit).	VBFO OFFSET HZ display is clocked until +5 V dc is applied at P1-84, when the clocking is ceased and the VBFO OFFSET HZ display is locked at the last frequency displayed.	Check U2C, U2B, U11C, and associated circuits.
(Cont)			

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
15. (Cont)	j. Stop rotating the TUNING knob.		
	k. Remove ground from P1-84.		
	l. Observe VBFO OFFSET HZ display.	VBFO OFFSET display should not change.	Same as step i.
16. Keep-alive checks	a. Front-panel controls set as follows: PWR to off. CONT to LCL. MODE to SSB/CW. BANDWIDTH to USB. DIAL to FINE. BFO to FIX. AGC to FAST. RF GAIN to full cw.		
	b. Disconnect external power from rear panel.		
	c. Discharge capacitors C14, C15, and C16 by temporarily placing a short across any one of them.		
	d. Connect +12-V dc power supply to external keep-alive; positive to TB3-4, negative to TB3-5.		
	e. Measure dc voltage at TP2.	+4.0 to +7.5 V dc.	Check CR3, Q16, and associated circuit.
	f. Remove external keep-alive supply from TB3.		
	g. Reconnect external power to rear panel.		
	h. Set PWR switch on.		
	i. Measure dc voltage at TP2.	+4.8 to +5.4 V dc.	Check VR1, Q3, and associated circuit.
	j. Set PWR switch off.		
	k. Disconnect external power from rear panel.		
	l. Discharge capacitors C14, C15, and C16.		
	m. Reconnect external power to rear panel.		
(Cont)	n. Set PWR switch on.		

Table 11. Control, Testing and Troubleshooting Procedures (Cont).

TEST	PROCEDURE	NORMAL INDICATION	IF INDICATION IS ABNORMAL
16. (Cont)	o. Note front-panel frequency reading.	000.00 kHz.	Check U29 thru U36 and associated circuit.
	p. Adjust front-panel TUNING knob for a 12 345.67 kHz frequency reading.		
	q. Set PWR switch off for several seconds.		
	r. Set PWR switch on.		
	s. Note front-panel frequency reading.	12 345.67 kHz.	Check C14, C15, C16, and associated circuit.
	t. Set PWR switch off.		
	u. Disconnect external power from rear panel for approximately 30 minutes.		
	v. Reconnect external power to rear panel.		
	w. Set PWR switch on.		
	x. Note front-panel frequency reading.	12 345.67 kHz.	Same as step 16.5.
17. Test complete	a. Set PWR switch off.		
	b. Disconnect external power from rear panel.		
	c. Remove control from extender and extender from unit.		
	d. Reinstall control in unit.		
	e. If removed in setup, reinstall parallel input, parallel output, and serial interface.		
	f. Reinstall top cover of unit.		

4. ALIGNMENT/ADJUSTMENT

4.1 Tuning Control

4.1.1 100-Hz Tuning Control

To provide 100-Hz tuning control, straps on the control must be positioned as shown in figure 7.

4.1.2 10-Hz Tuning Control

To provide 10-Hz tuning control, straps on the control must be positioned as shown in figure 7.

4.2 RF Filter Control

4.2.1 Standard Filters

To provide rf filter control when using standard rf bandpass, filtering, straps on control must be positioned as shown in figure 8.

4.2.2 1/2-Octave Filtering

To provide rf filter control when using 1/2-octave filtering, straps on control must be positioned as shown in figure 8.

5. REPAIR

Repair of the control card is accomplished using standard maintenance and planar card repair procedures. Refer to the maintenance section of this instruction book for planar card repair procedures.

6. PARTS LIST/DIAGRAMS

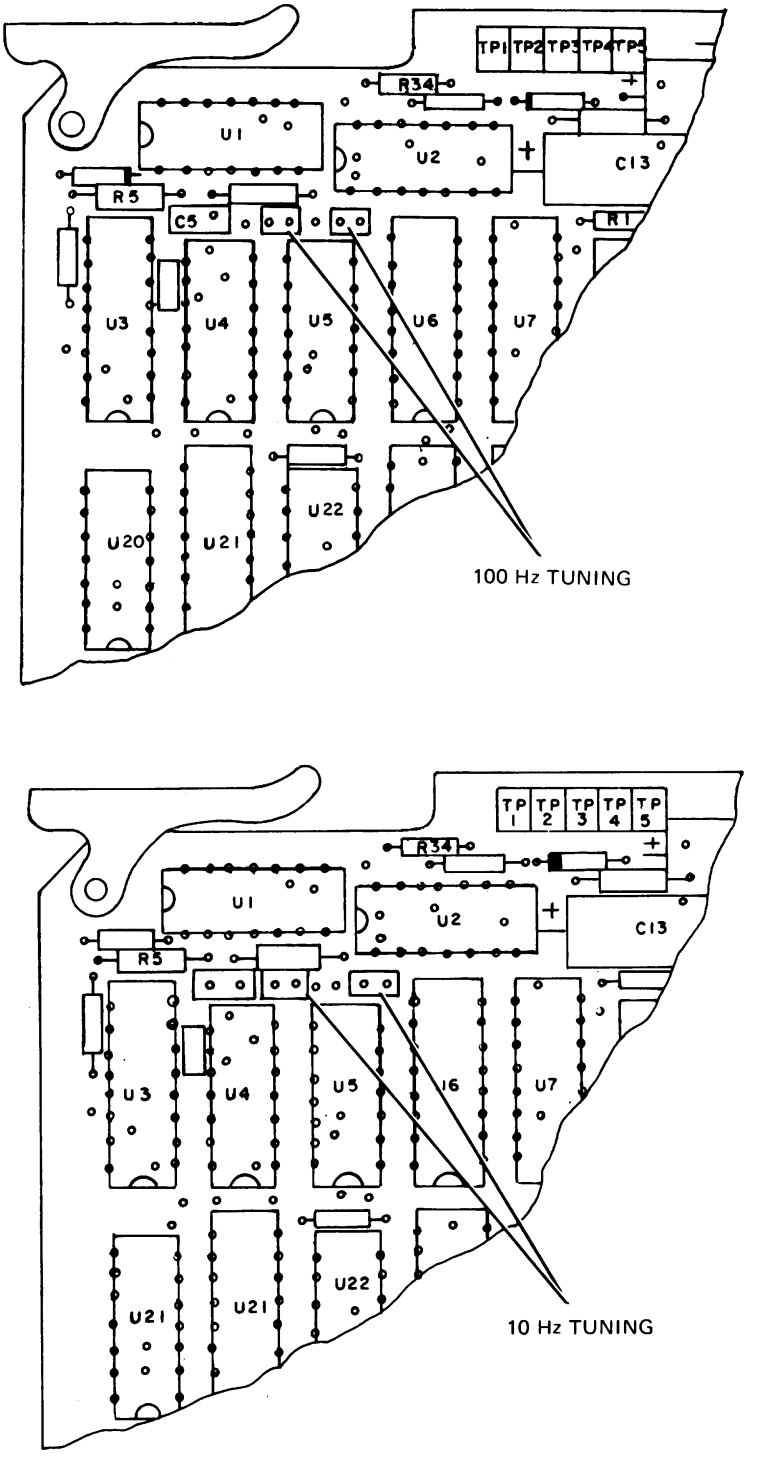
This paragraph assists in identification, requisition, and issuance of parts and in maintenance of the equipment. A parts location illustration, schematic diagram, parts list tabulation, and modification history are included in the schematic diagram, figure 9. The parts location illustration is a design engineering drawing that shows exact component placement on the circuit cards.

Use the reference designator indicated on schematic and parts location diagram to locate parts in the parts list tabulation. The Collins part number and description are listed for each reference designator.

Modifications are identified by an alphanumeric identifier assigned to each design change. These identifiers are referenced in the DESCRIPTION column of the parts list in parentheses and on the schematic diagram inside an arrow that points to the change. Each change relates to the revision identifier (REV) stamped on the circuit card/subassembly and is listed in the EFFECTIVITY column of the modification history.

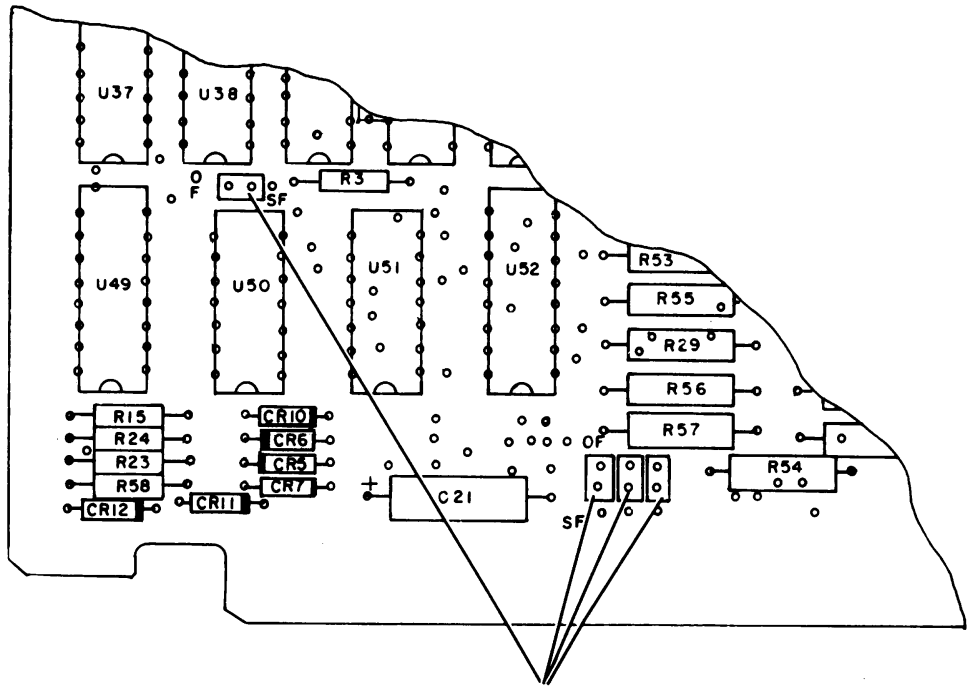
Listed below are the circuit cards/subassemblies with the latest effectivity covered by these instructions.

CIRCUIT CARD/ SUBASSEMBLY	COLLINS PART NUMBER	LATEST EFFECTIVITY
Control	638-6065-001	REV D

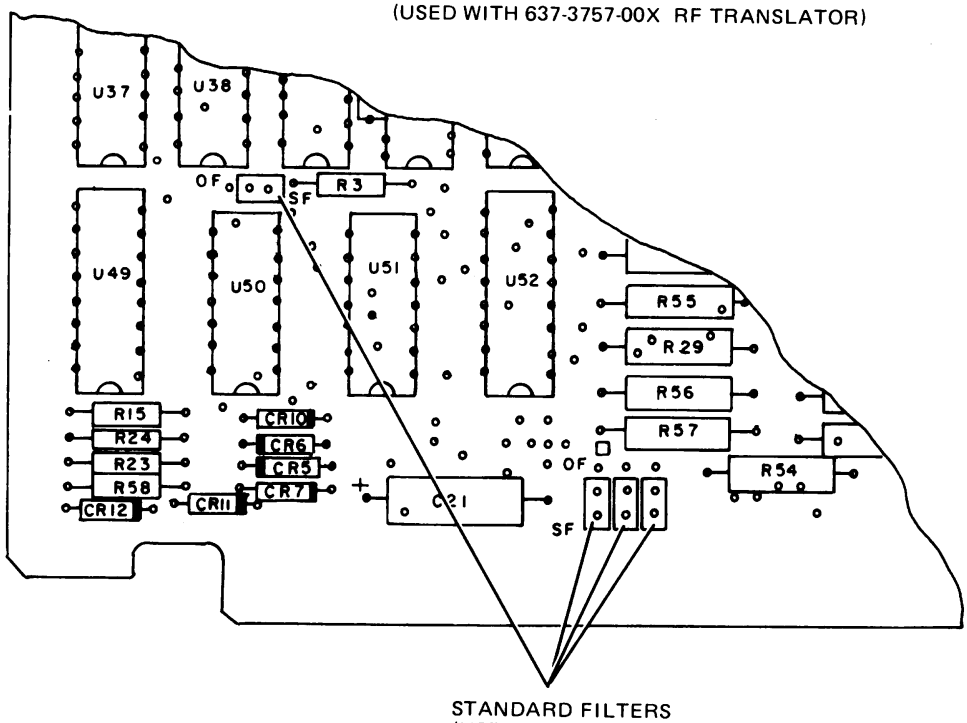


TPA-0849-019

Strapping for Tuning Control
Figure 7



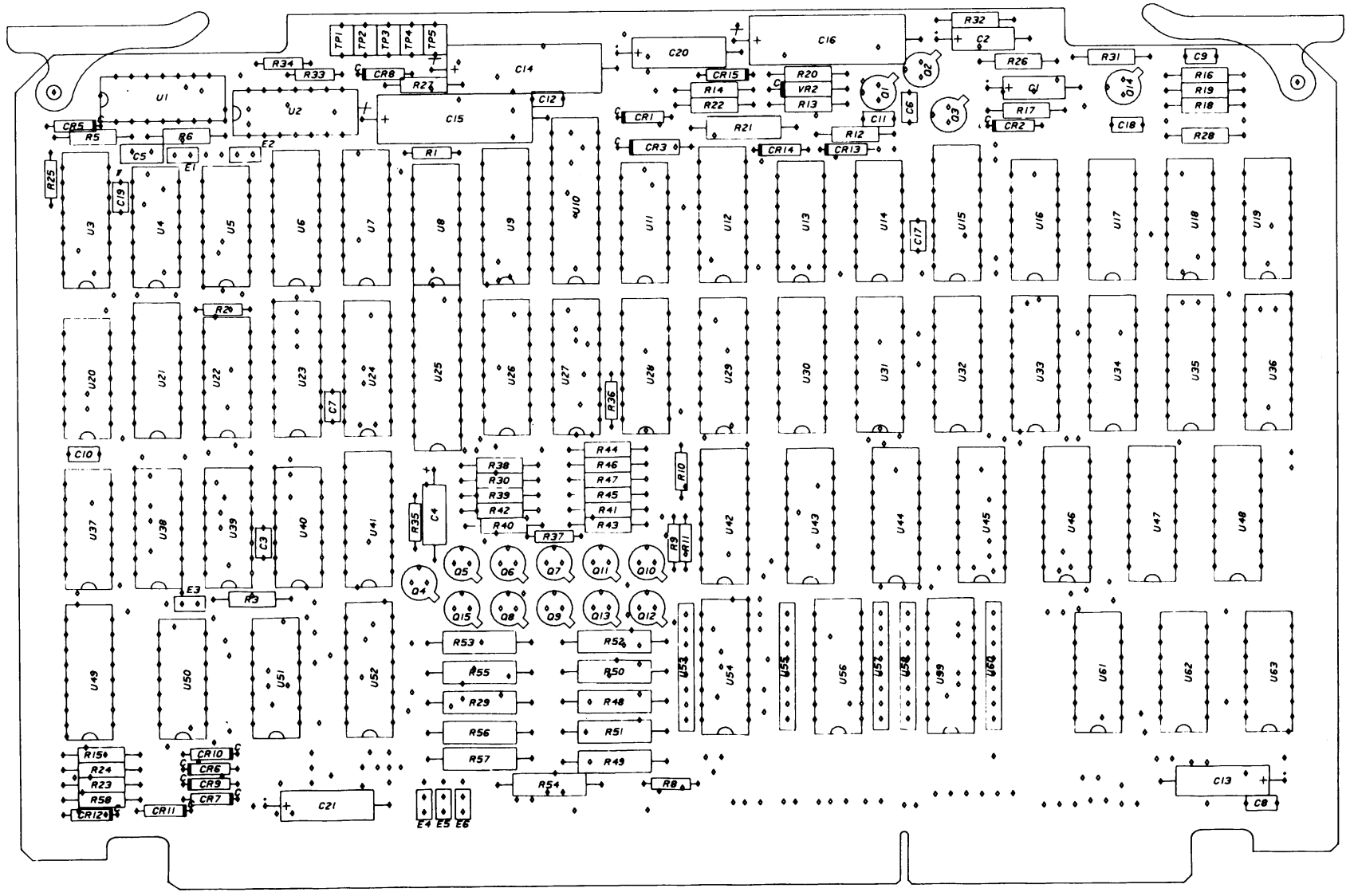
½ OCTAVE FILTERS
(USED WITH 637-3757-00X RF TRANSLATOR)



STANDARD FILTERS
(USED WITH 637-1767-00X RF TRANSLATOR)

TPA-0850-019

Strapping for Rf Filter Control
Figure 8



TPA-0903-014

Control, Schematic Diagram
Figure 9 (Sheet 1 of 6)

PARTS LIST

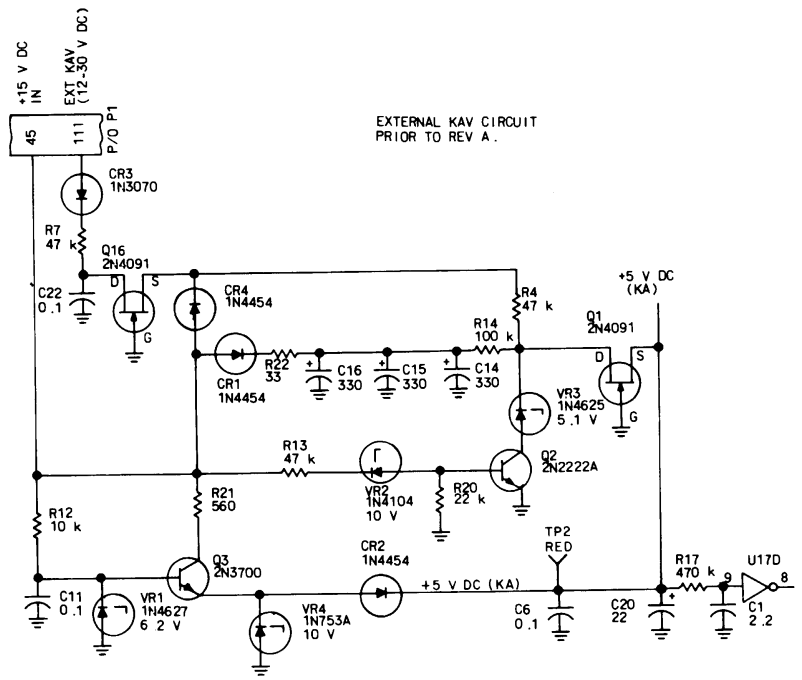
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
	CONTROL	638-6065-001	
CR1,CR2	SEMICOND DEVICE 1N4454	353-3644-010	
CR3	SEMICOND DEVICE 1N3070	353-3083-000	
CR4	SEMICOND DEVICE 1N4454 (A1)	353-3644-010	
CR5-CR12	SEMICOND DEVICE 1N4454	353-3644-010	
CR13-CR15	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V (A1)	913-5019-200	
C1,C2	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C3	CAPACITOR,FXD CER DIEL, 1000PF, 10%, 200V	913-4018-000	
C4	CAPACITOR,FXD ELCTLT, 2.2UF, 10%, 20V	184-9086-430	
C5	CAPACITOR,FXD MICA DIEL, 68PF, 5%, 50V	912-4141-330	
C6-C12	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C13	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C14-C16	CAPACITOR,FXD ELCTLT, 330UF, PORM20%, 20V	184-9117-040	
C17-C19	CAPACITOR,FXD CER DIEL, 0.01UF, 10%, 100V	913-5019-200	
C20	CAPACITOR,FXD ELCTLT, 22UF, 10%, 15V	184-9086-310	
C21	CAPACITOR,FXD ELCTLT, 15UF, 10%, 20V	184-9086-490	
Q1	TRANSISTOR 2N4091	352-0759-010	
Q2	TRANSISTOR 2N2222A	352-0661-020	
Q3	TRANSISTOR 2N2222A	352-0661-020	
Q4-Q13	TRANSISTOR 2N2907A	352-0551-010	
Q14	TRANSISTOR 2N2222A	352-0661-020	
Q15	TRANSISTOR 2N2907A	352-0551-010	
Q16	TRANSISTOR 2N4091(A1)	352-0759-010	
R1	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R2	RESISTOR,FXD CMPSN, 100K, 10%, 1/8W	745-2413-000	
R3	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R4	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R5	RESISTOR,FXD FILM, 88.7K, 1%, 1/8W	705-3605-930	
R6	RESISTOR,FXD FILM, 178K, 1%, 1/8W	705-1104-000	
R7	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R8-R11	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/8W	745-2449-000	
R12	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W (A1)	745-0785-000	
R12	RESISTOR,FXD CMPSN, 27K, 10%, 1/4W	745-0800-000	
R13	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W (A1)	745-0809-000	
R13	RESISTOR,FXD CMPSN, 33K, 10%, 1/4W	745-0803-000	
R14	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W (A1)	745-0821-000	
R14	RESISTOR,FXD CMPSN, 47K, 10%, 1/4W	745-0809-000	
R15	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
R16	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R17,R18	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R19	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R20	RESISTOR,FXD CMPSN, 22K, 10%, 1/4W (A1)	745-0797-000	
R20	RESISTOR,FXD CMPSN, 10K, 10%, 1/4W	745-0785-000	
R21	RESISTOR,FXD CMPSN, 560 OHMS, 10%, 1/2W (A1)	745-1342-000	
R21	RESISTOR,FXD CMPSN, 6.8K, 10%, 1/2W	745-1387-000	
R22	RESISTOR,FXD CMPSN, 33 OHMS, 10%, 1/4W	745-0695-000	
R23,R24	RESISTOR,FXD CMPSN, 1MEGO, 10%, 1/4W	745-0857-000	
R25,R26	RESISTOR,FXD CMPSN, 0.47MEGO, 10%, 1/4W	745-0845-000	
R27,R28	RESISTOR,FXD CMPSN, 0.22MEGO, 10%, 1/4W	745-0833-000	
R29	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R30	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W	745-0761-000	
R31	RESISTOR,FXD CMPSN, 15K, 10%, 1/4W	745-0791-000	
R32	RESISTOR,FXD CMPSN, 0.22MEGO, 10%, 1/4W	745-0833-000	
R33,R34	RESISTOR,FXD CMPSN, 470K, 10%, 1/8W	745-2437-000	
R35-R37	RESISTOR,FXD CMPSN, 22K, 10%, 1/8W	745-2389-000	
R38-R47	RESISTOR,FXD CMPSN, 2.2K, 10%, 1/4W	745-0761-000	
R48	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/2W	745-1359-000	
R49	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R50	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/2W	745-1359-000	
R51	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R52-R55	RESISTOR,FXD CMPSN, 1.5K, 10%, 1/2W	745-1359-000	
R56,R57	RESISTOR,FXD 1.5K, 1%, 1W	747-1499-591	
R58	RESISTOR,FXD CMPSN, 0.10MEGO, 10%, 1/4W	745-0821-000	
TP1	JACK,TIP BRN	360-0484-070	
TP2	JACK,TIP RED	360-0484-020	
TP3	JACK,TIP ORN	360-0484-050	
TP4	JACK,TIP YEL	360-0484-060	
TP5	JACK,TIP GRN	360-0484-040	
U1	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U2	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U3	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
U4	INTEGRATED CIRCUIT 4013BPC	351-8159-110	
U5	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U6	INTEGRATED CIRCUIT 4040BPC	351-8159-240	
U7	INTEGRATED CIRCUIT F4051PC	351-8227-010	
U8	INTEGRATED CIRCUIT MC14071BCP	351-8287-010	
U9	INTEGRATED CIRCUIT 4050BPC	351-8159-220	
U10	PROM, BAND DECODER	614-0133-013	
U11	INTEGRATED CIRCUIT MC14081BCP	351-8287-030	
U12	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U13	INTEGRATED CIRCUIT MC14070BCP	351-8407-010	
U14	INTEGRATED CIRCUIT 4016BPC	351-8159-070	
U15	INTEGRATED CIRCUIT MC14528BCP	351-8421-020	
U16	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U17	INTEGRATED CIRCUIT MC14069UBPC	351-8287-080	
U18	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U19,U20	INTEGRATED CIRCUIT 4011BFC	351-8159-340	
U21	INTEGRATED CIRCUIT MC14016BCP	351-8253-010	
U22	INTEGRATED CIRCUIT 4011BPC	351-8159-340	
U23	INTEGRATED CIRCUIT F4049BFC	351-8159-210	
U24	INTEGRATED CIRCUIT F4051PC	351-8227-010	
U25	PROM,RATE DECODER (A2)	614-0133-010	

PARTS LIST (Cont)

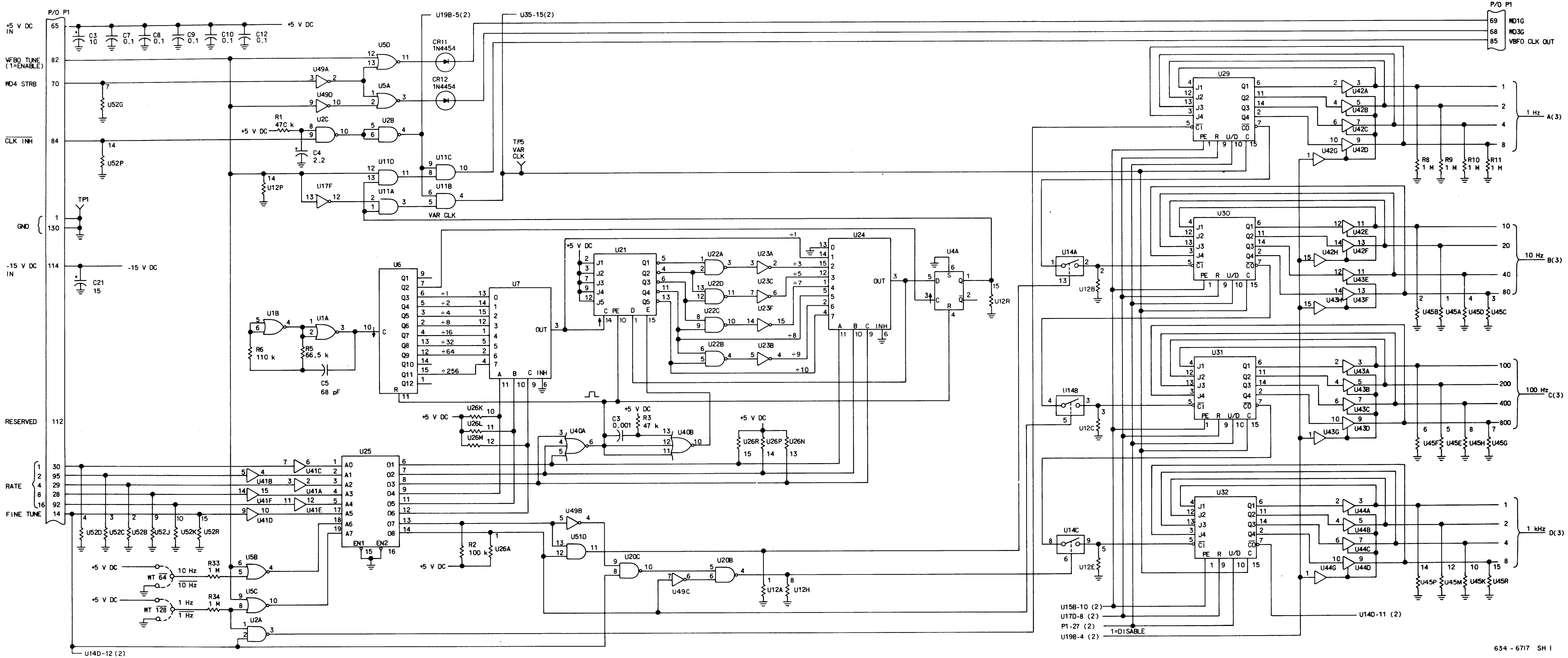
REF DES	DESCRIPTION	COLLINS PART NUMBER	USABLE ON CODE
U25	PROM,RATE DECODER	614-0133-012	
U26	RESISTOR NTWK 100K, 5%, 1.25W PKG	350-4030-130	
U27,U28	INTEGRATED CIRCUIT F4049BPC	351-8159-210	
U29-U36	INTEGRATED CIRCUIT CD4510BCN	351-8497-010	
U37	INTEGRATED CIRCUIT 4001BPC	351-8159-320	
U38	INTEGRATED CIRCUIT MC14071BCP	351-8287-010	
U39	INTEGRATED CIRCUIT MC14081BCP	351-8287-030	
U40	INTEGRATED CIRCUIT 4025BPC	351-8159-370	
U41	INTEGRATED CIRCUIT 4050BPC	351-8159-220	
U42-U44	INTEGRATED CIRCUIT MC14503BCP	351-8490-010	
U45	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U46	INTEGRATED CIRCUIT MC14503BCP	351-8490-010	
U47	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U48	INTEGRATED CIRCUIT MC14503BCP	351-8490-010	
U49	INTEGRATED CIRCUIT F4049BFC	351-8159-210	
U50	INTEGRATED CIRCUIT MC14071BCP	351-8287-010	
U51	INTEGRATED CIRCUIT MC14081BCP	351-8287-030	
U52	RESISTOR NTWK 1M, 5%, 1.25W PKG	350-4030-150	
U53	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U54	INTEGRATED CIRCUIT CA3081	351-7802-020	
U55	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U56	INTEGRATED CIRCUIT CA3081	351-7802-020	
U57,U58	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U59	INTEGRATED CIRCUIT CA3081	351-7802-020	
U60	RESISTOR NTWK FILM, 15K, 2%, 1W	350-4046-770	
U61-U63	INTEGRATED CIRCUIT MC14069BCP	351-8287-080	
VR1	SEMICOND DEVICE 1N4627(A1)	353-3591-510	
VR2	SEMICOND DEVICE IN4104	353-3591-060	
VR3	SEMICOND DEVICE 1N4625(A1)	353-3591-490	
VR4	SEMICOND DEVICE 1N758A(A1)	353-2724-000	

MODIFICATION HISTORY

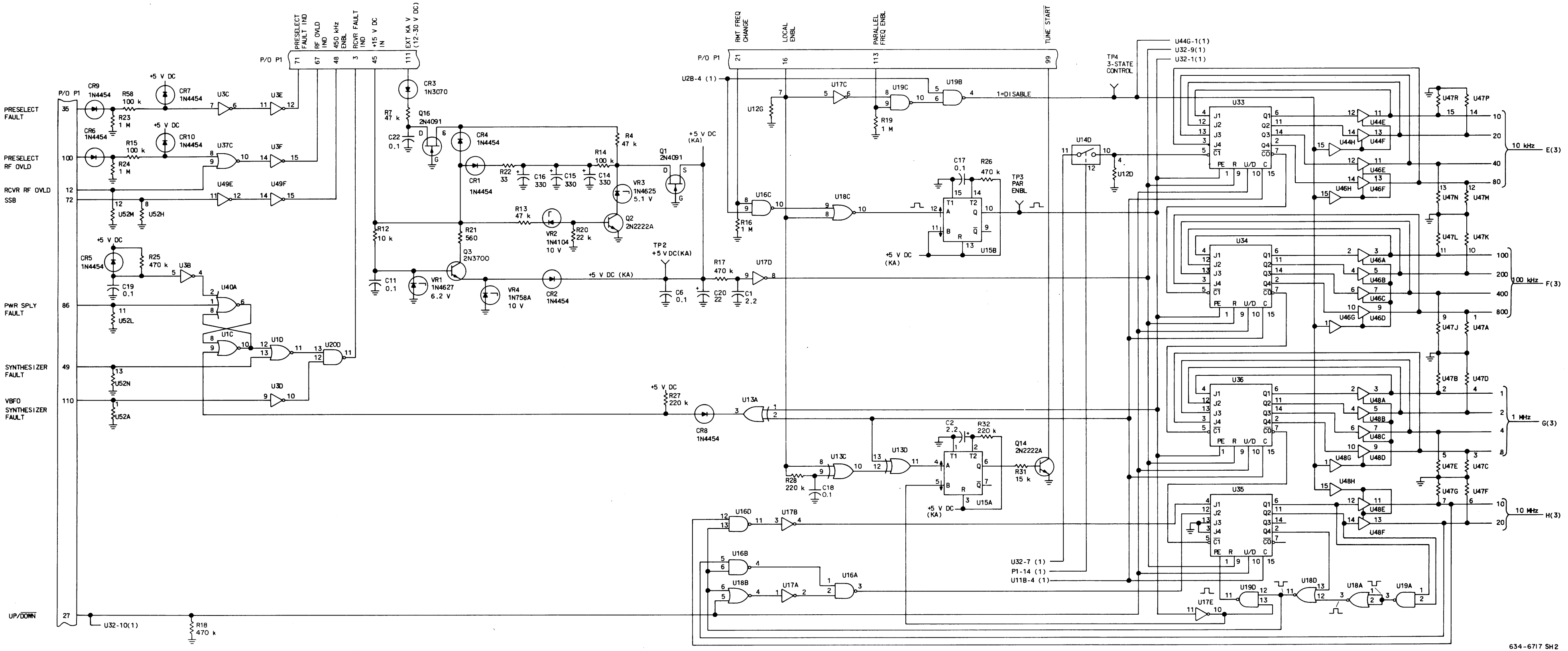
REVISION IDENT	DESCRIPTION OF REVISION AND REASON FOR CHANGE	EFFECTIVITY
A1	External KAV (keep-alive voltage) circuit changed. Circuit was as shown in diagram below. Deleted: CR4, 1N4454. C22, 0.01 μF. Q16, 2N4091. R4, 47 kΩ. R7, 47 kΩ VR1, 1N4627. VR3, 1N4625. VR4, 1N758A. Changed: Q3 from 2N3700 to 2N2222A. R12 from 10 kΩ to 27 kΩ. R13 from 47 kΩ to 33 kΩ. R14 from 100 kΩ to 47 kΩ. R20 from 22 kΩ to 10 kΩ. R21 from 560 Ω to 6800 Ω. Added: CR13, 1N4454. CR14, 1N4454. CR15, 1N4454.	REV A and above
A2	Changed PROM U25 (Tuning Rate Decoder) from 614-0133-010 to 614-0133-012.	REV C and above



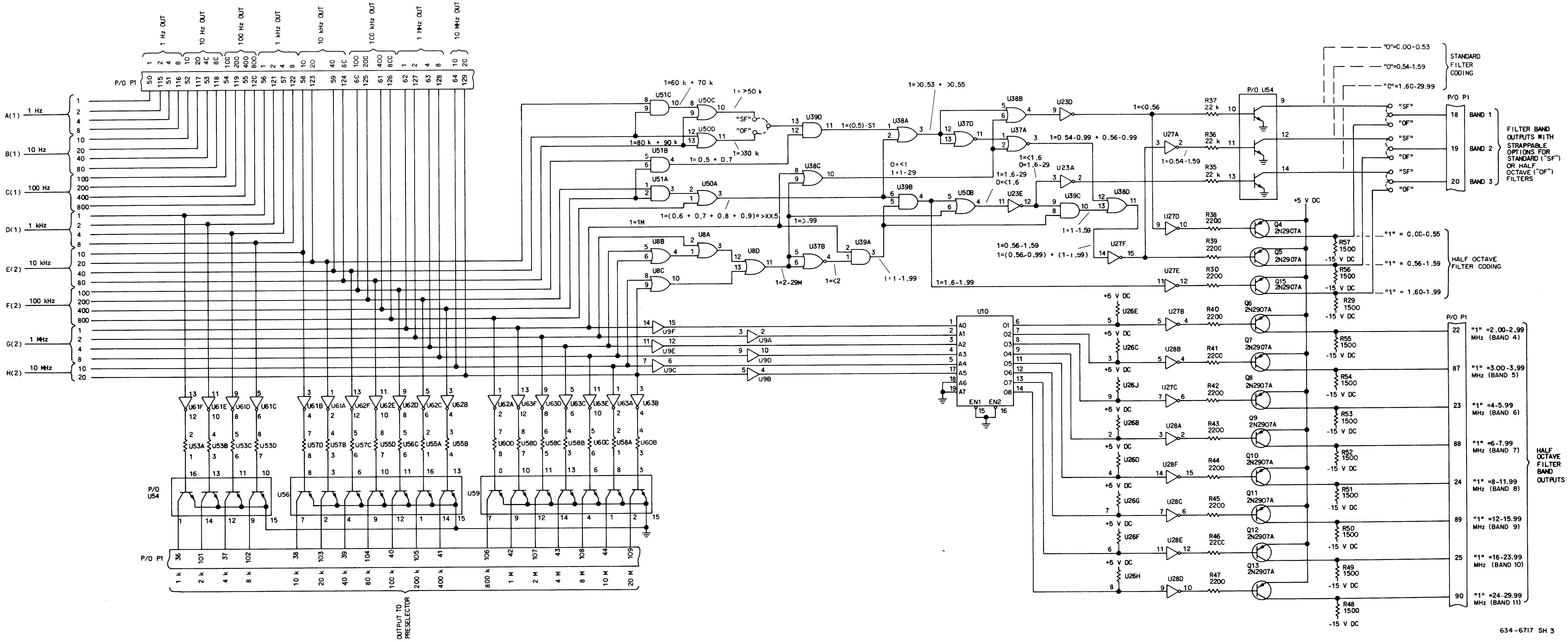
Control, Schematic Diagram
Figure 9 (Sheet 2)



Control, Schematic Diagram
Figure 9 (Sheet 3)



Control, Schematic Diagram
Figure 9 (Sheet 4)



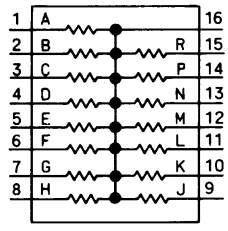
Control, Schematic Diagram
Figure 9 (Sheet 5)

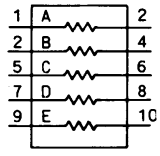
NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

3. U12, U45, U47, U52 (1 M)
   U26 (100 k)
   U53, U55, U57
   U58, U60 (15 k)





4. NONSTANDARD ABBREVIATION
   KA-KEEP ALIVE

MICROCIRCUIT INFORMATION

	U NO.	TYPE	PWR (V DC) +5	PWR (V DC) +5 KA	PWR (V DC) GND	SPARE SECTIONS
	U1	F4001BPC	14		7	
	U2	F4011BPC		14	7	D
	U3	F4049BPC	1		8	
	U4	F4013BPC	14		7	B
	U5	R4C01BPC	14		7	
	U6	F4040BPC	16		8	
	U7	F4C51PC	16		7,8	
	U8	MC14071BCP	14		7	
	U9	F4C5CPC	1		8	
*	U10	74S471	20		10	
	U11	MC14081BCP		14	7	
	U12	NOTE 3			16	F, J, L, M,N
	U13	MC14C70BCP		14	7	B
	U14	F4016BPC		14	7	
	U15	MC14528BCP		16	8	
	U16	F4011BPC		14	7	
	U17	MC14069BCP		14	7	
	U18	F4001BPC		14	7	
	U19	F4011BPC		14	7	
	U20	F4011BPC	14		7	A
	U21	MC14018BCP	16		8	
	U22	F4011BPC	14		7	
	U23	F4049BPC	1		8	
	U24	F4051PC	16		7,8	
(A1) **	U25	74S471	20		10	
	U26	NOTE 3	16			
	U27	F4049BPC	1		8	
	U28	F4049BPC	1		8	
	U29	CD4510BCN		16	8	
	U30	CD4510BCN		16	8	
	U31	CD4510BCN		16	8	
	U32	CD4510BCN		16	8	

U NO.	TYPE	PWR (V DC) +5	PWR (V DC) +5 KA	PWR (V DC) GND	SPARE SECTIONS
U33	CD4510BCN		16	8	
U34	CD4510BCN		16	8	
U35	CD4510BCN		16	8	
U36	CD4510BCN		16	8	
U37	F4001BPC	14		7	
U38	MC14071BPC	14		7	
U39	MC14081BCP	14		7	
U40	F4025BPC	14		7	
U41	F4050PC	1		8	
U42	MC14503BCP		16	8	
U43	MC14503BCP		16	8	
U44	MC14503BCP		16	8	
U45	NOTE 3			16	J, L, N
U46	MC14503BCP		16	8	
U47	NOTE 3			16	H
U48	MC14503BCP		16	8	
U49	F4049BPC	1		8	
U50	MC14071BCP	14		7	
U51	MC14081BCP	14		7	
U52	NOTE 3			16	
U53	NOTE3				
U54	CA3C81			5	
U55	NOTE 3				
U56	CA3081			5	
U57	NOTE 3				A
U58	NOTE 3				
U59	CA3081			5	
U60	NOTE 3				A
U61	MC14069BCP	14		7	
U62	MC14069BCP	14		7	
U63	MC14069BCP	14		7	

* PROM, BAND DECODER, PROGRAMMED PN 614-0133-013.

(A1) ** PROM, TUNING RATE DECODER, PROGRAMMED PN 614-0133-012.

634-6717 SH 4

Control, Schematic Diagram
Figure 9 (Sheet 6)